From The Lab to The Fab: Transistors to Integrated Circuits

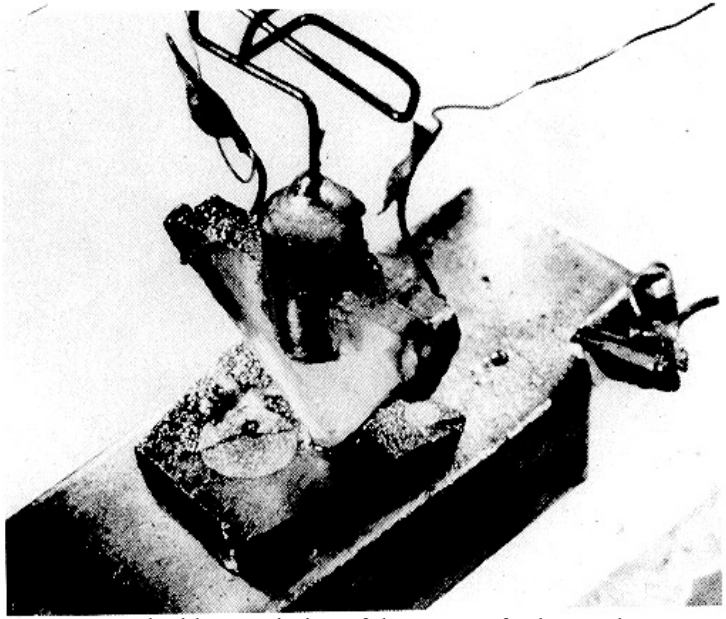
Howard R. Huff

International SEMATECH
Austin, TX 78741

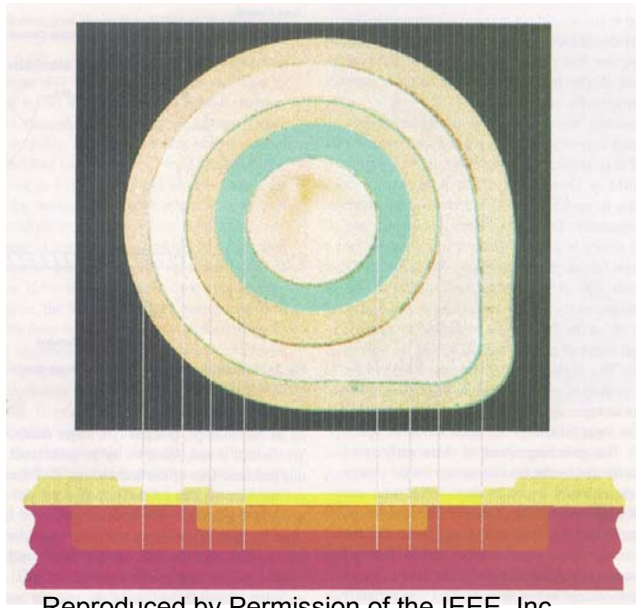
Agenda

- Introduction
- Threshold events
- Transistor Fabrication
  - Point-contact
  - Grown-junction
  - Alloy formation
  - Diffusion
- Mesa and planar advances
- Integrated circuit beginnings
- Bipolar and DRAM IC Issues
  - (1960-1980's)
- Prognosis
- Acknowledgements

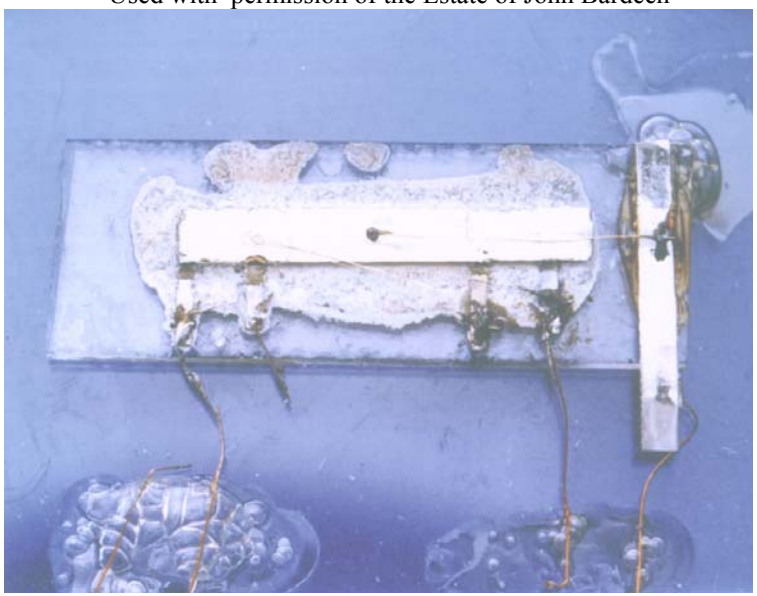
Transistors to Integrated Circuits



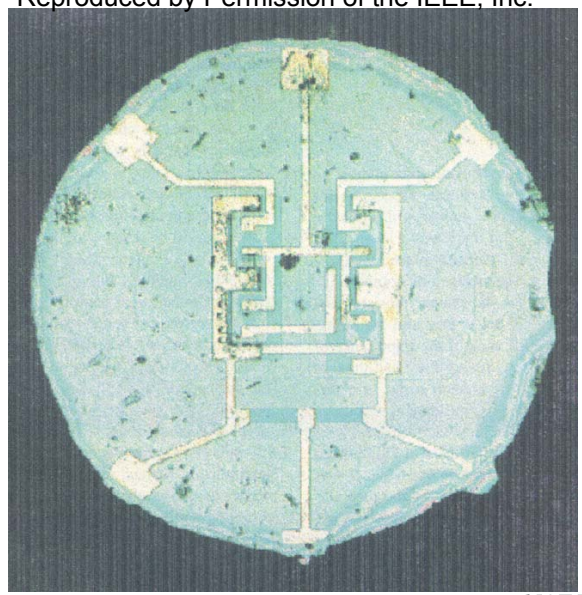
Used with permission of the Estate of John Bardeen



Reproduced by Permission of the IEEE, Inc.



Courtesy of Texas Instruments, Inc.

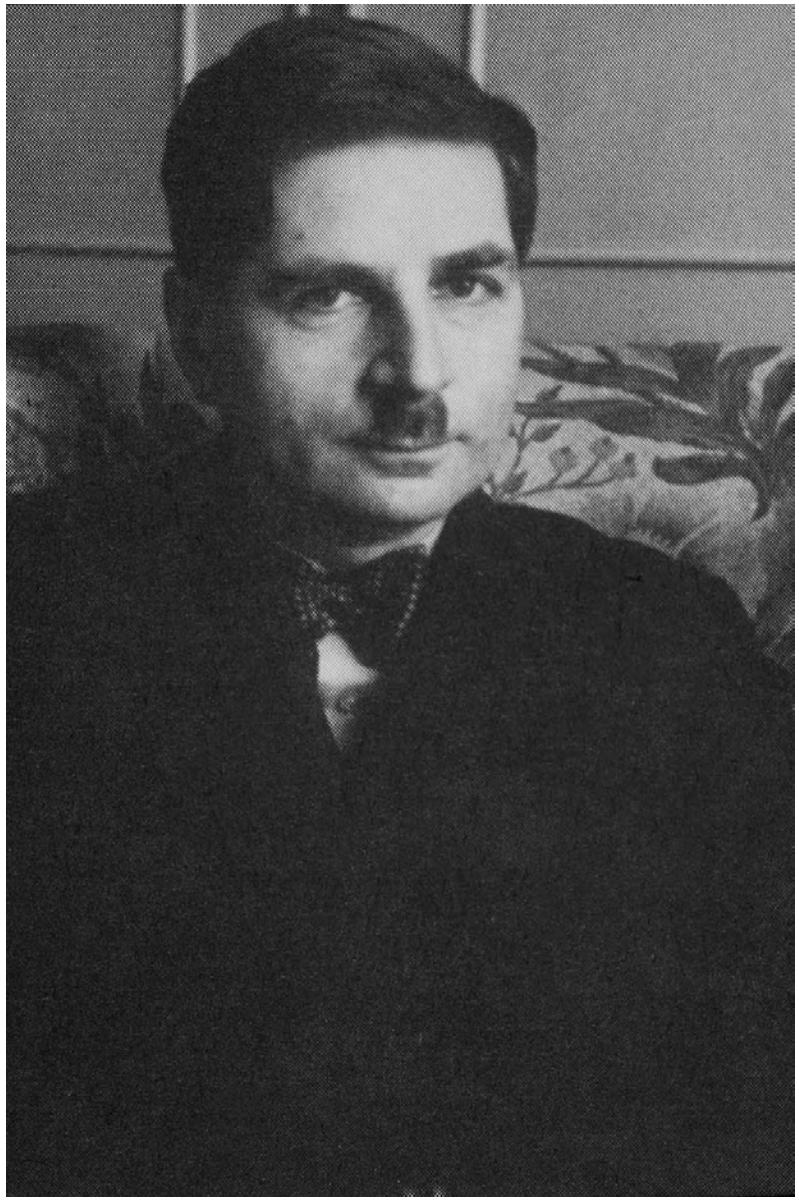


Reproduced by Permission of the IEEE, Inc.

Nevill Mott

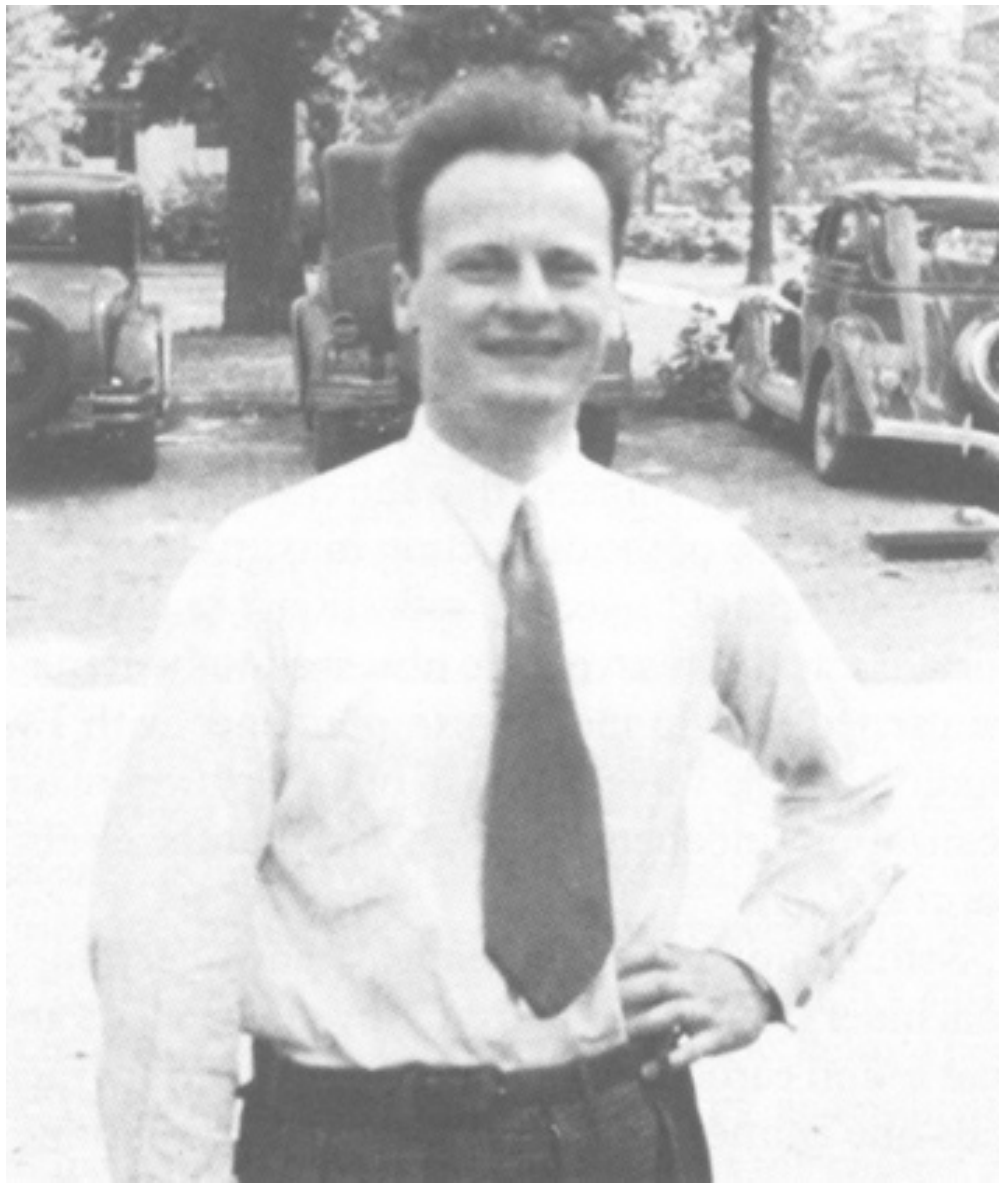
Courtesy of Fred Seitz

Walter Schottky



Courtesy of Fred Seitz

Hans Bethe (Ann Arbor, 1935)



Courtesy of Lillian Hoddeson

Fabrication of Metallurgical Grade Ge and Si

- **Conversion of Ge and Si ores to metallurgical-grade material and their subsequent purification by Fred Seitz in conjunction with Dupont**
  - **$Zn + SiCl_4 \Rightarrow Si + ZnCl_4$ (vapor phase reaction)**
  - **Purity to about 1 part in 10^5**

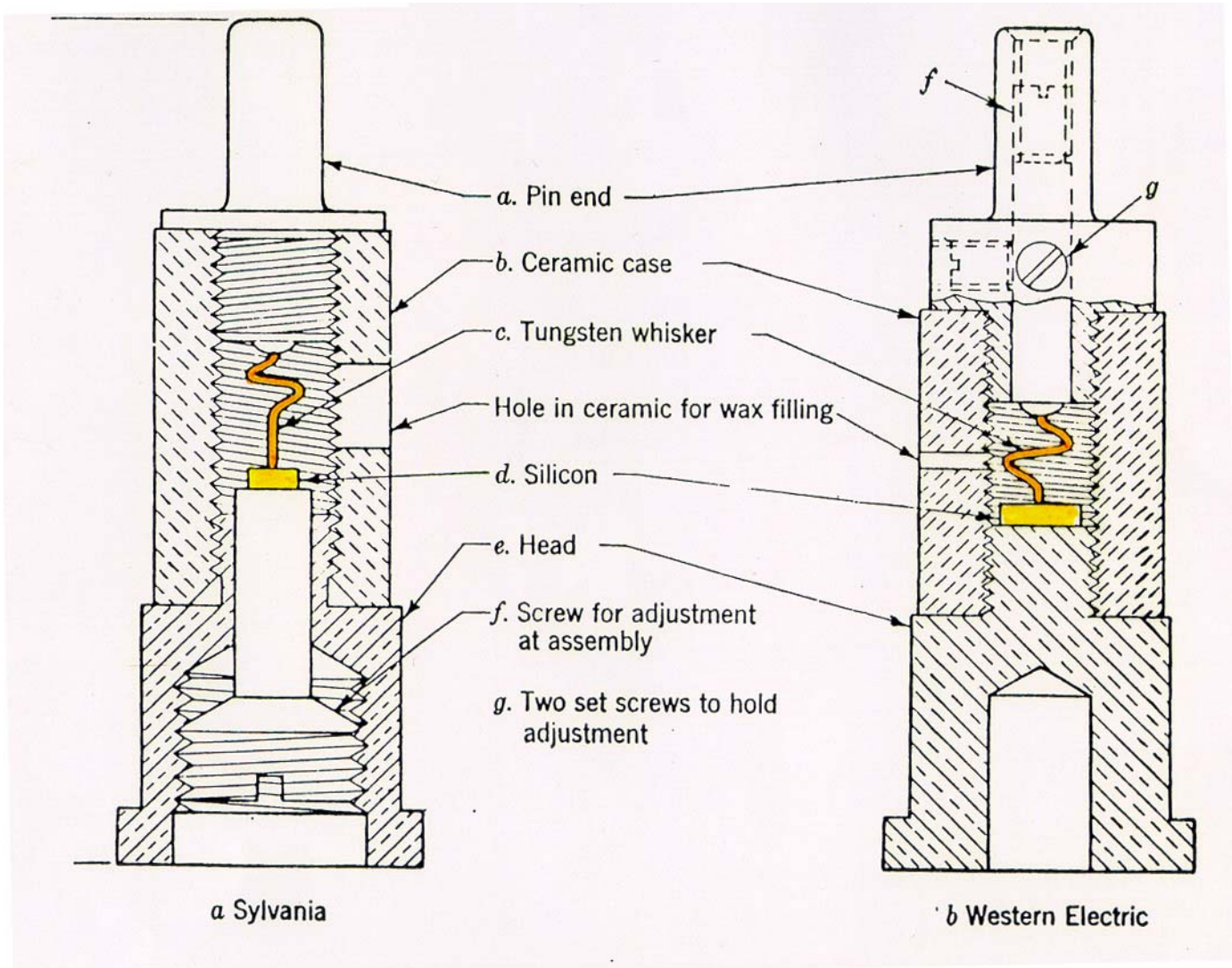
Fred Seitz

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

C. Marcus Olson (center)

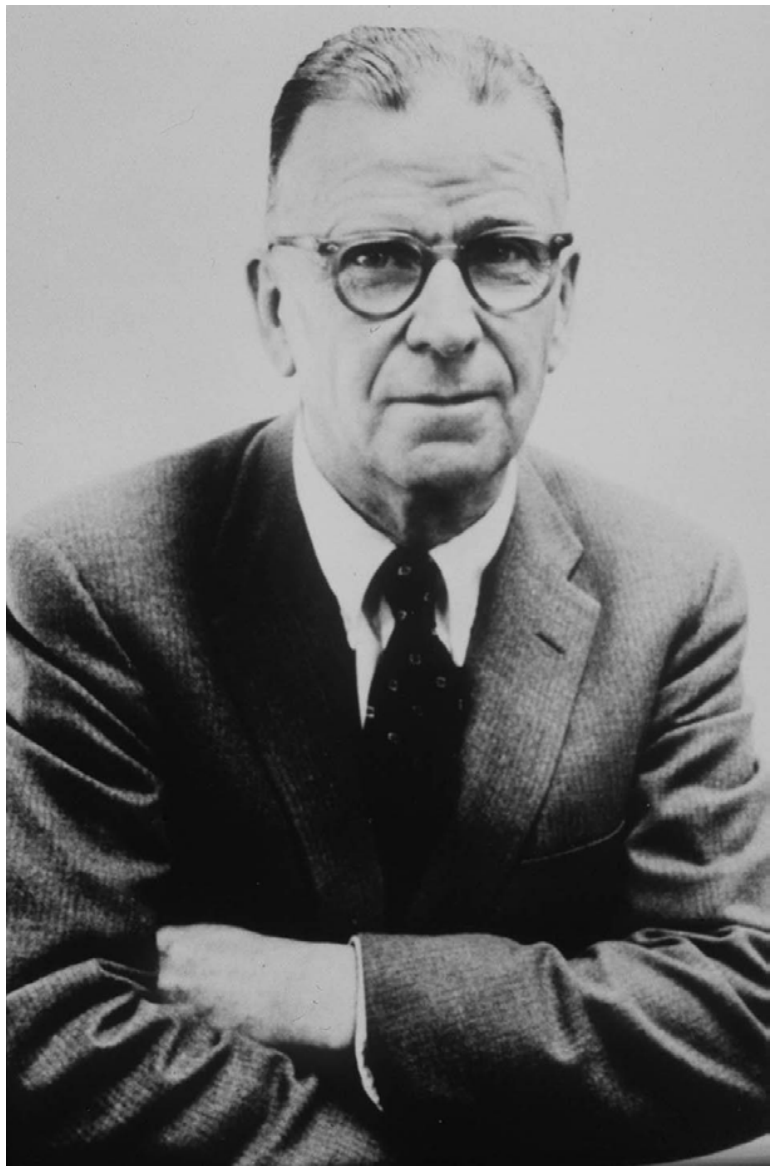
Courtesy of Fred Seitz

Crystal Rectifiers For Radar in WW II



After Michael Riordan
(Torrey and Whitmer)

Mervin Kelly

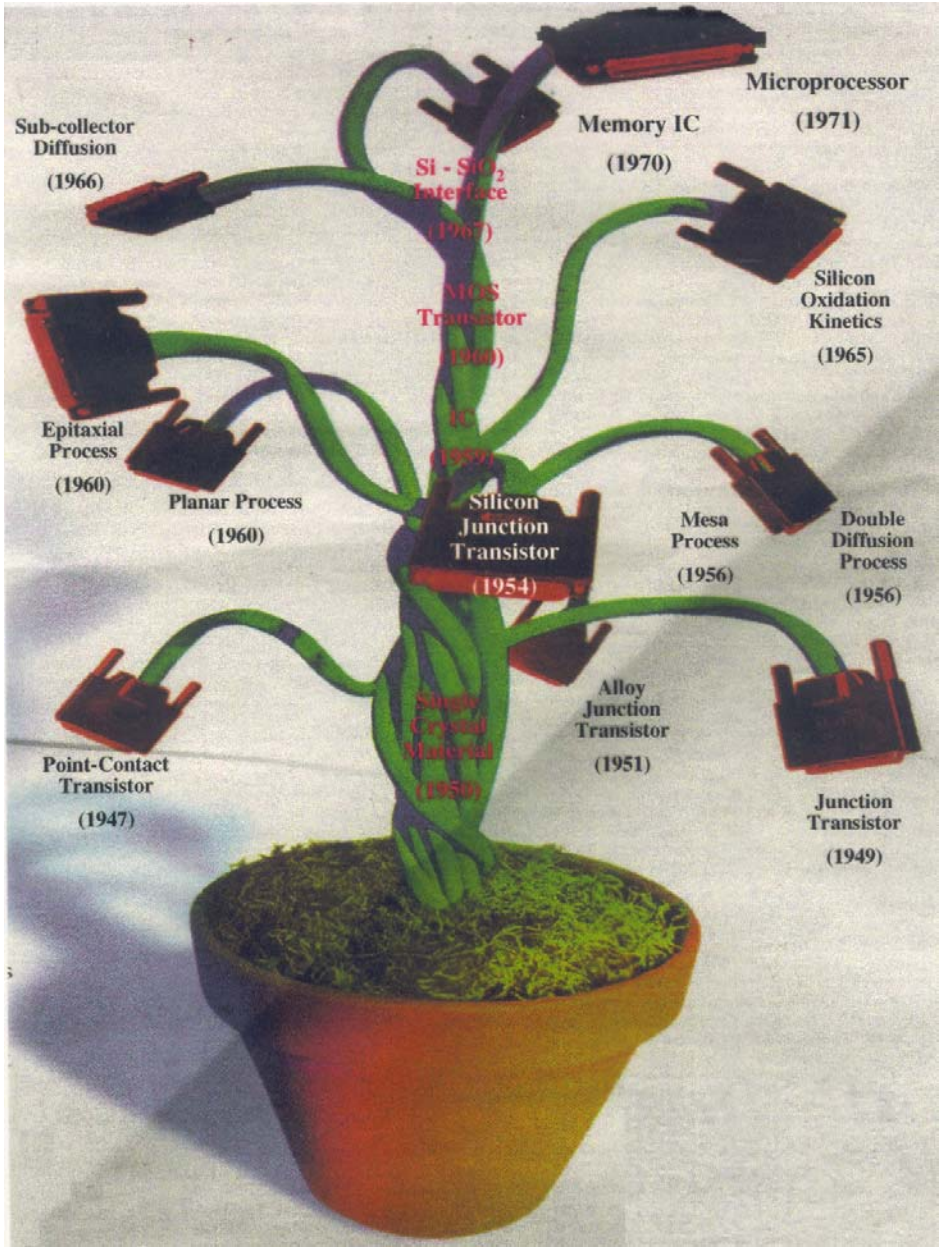


Courtesy of Fred Seitz

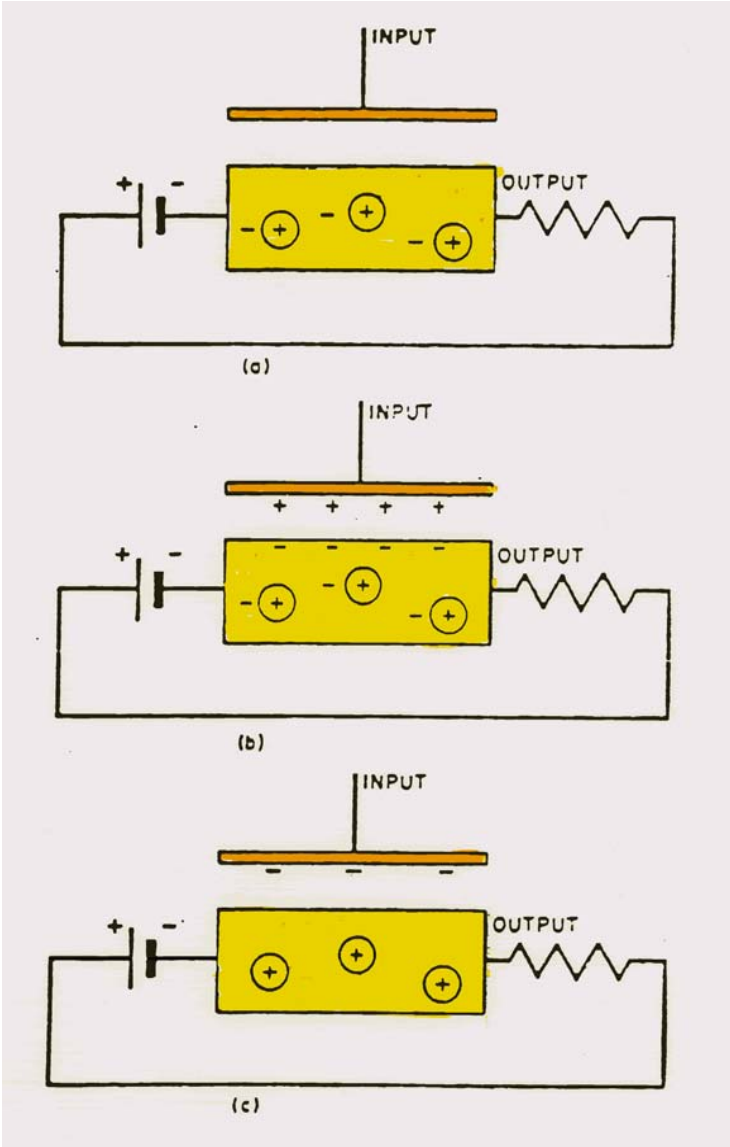
John Bardeen

Courtesy of Lillian Hoddeson

Tree of Growth

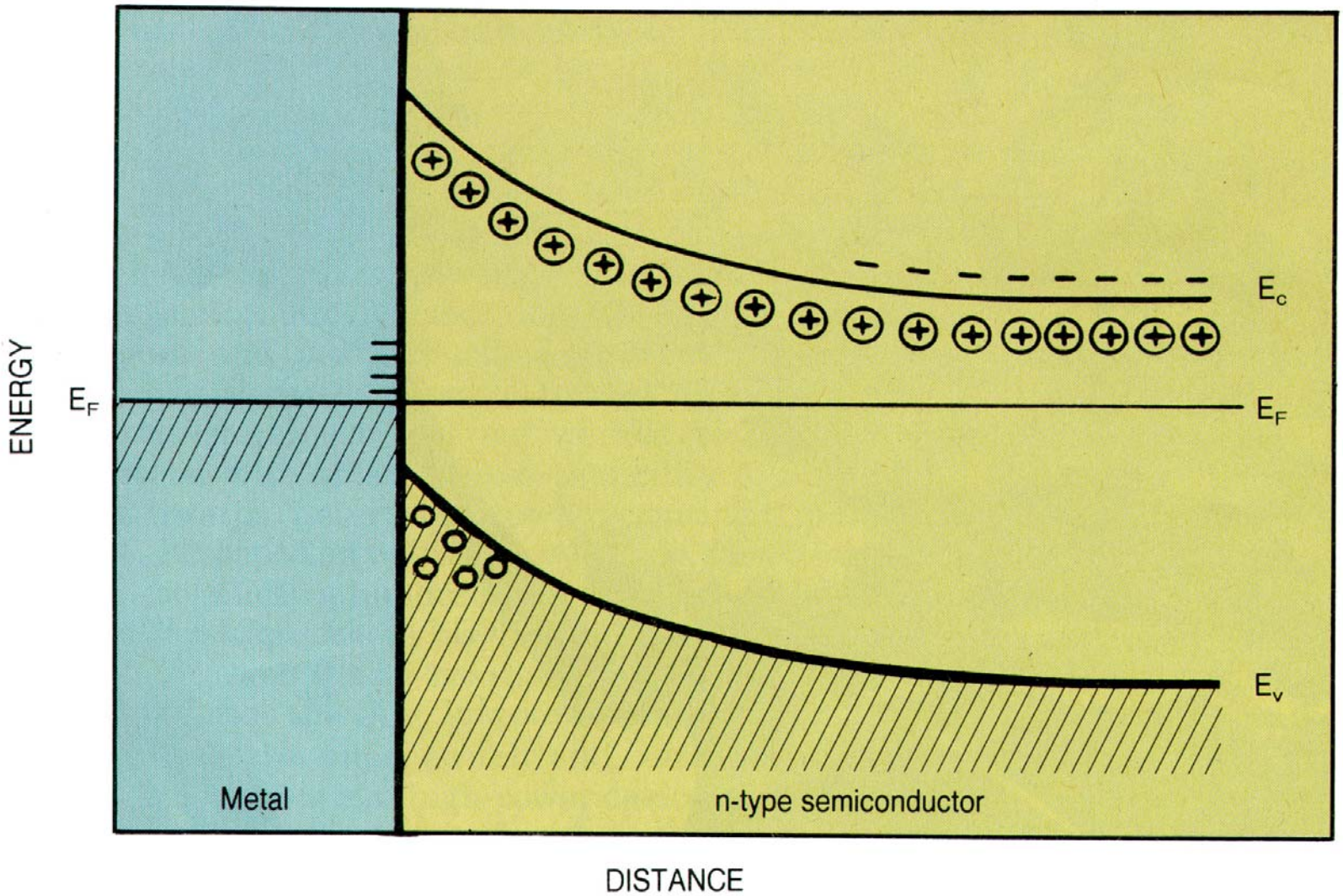


Shockley's Field-Effect Experiment



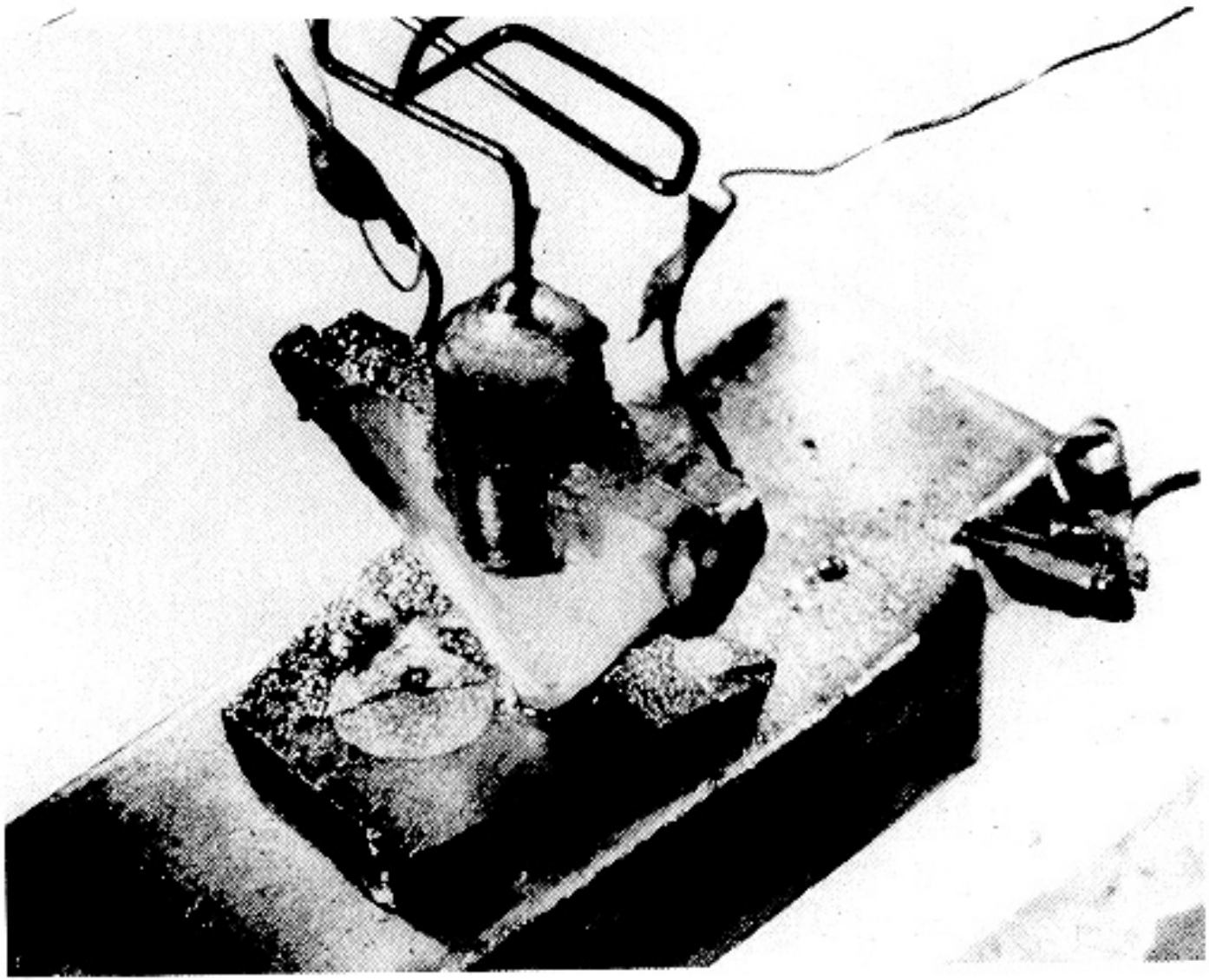
After W. Shockley, *Path to The Conception of The Junction Transistor*, IEEE Trans. Electron Devices, **ED-23**, 597-620 (1976), reprinted in **ED-31**, 1523-1546 (1984) © 1984 IEEE

Energy -Level Diagram For Metal / N-Type Semiconductor With Surface States



After Nick Holonyak

Historic Day: December 16, 1947 (con't)



Used with permission of the Estate of John Bardeen

The Press Announcement - July 1, 1948

The News of Radio

Two New Shows on CBS Will Replace 'Radio Theatre' During the Summer

Two new shows are announced by CBS to serve as summer replacements for the hour-long "Radio Theatre" on Monday evenings. The first, to be heard at 9:30 P. M., will be "Mr. Tutt," based on the stories of the late Arthur Train. Willard Wright will have the title role and Arnold Perl will do the adaptations. It will make its debut next week.

The second, to open on July 12, will be "Our Miss Brooks," with Eve Arden playing the role of a school teacher who encounters a variety of adventures. It will be written by Al Lewis and Lee Loeb, with Larry Berns serving as director. "Our Miss Brooks" will be offered at 9 P. M. Mondays.

A situation comedy with musical overtones, headlined by Mel Torme, has been selected as the replacement for the Dinah Shore-Harry James program at 8 P. M. Tuesdays over NBC, starting next week. The supporting company will include Janet Waldo and John Brown. Harmon Alexander and Ben Perry will do the script. Frank Dannig will be the producer and Ben Elliott, the musical director.

Station WFUV, Fordham University's frequency modulation outlet, will observe the completion of its first year of operation today. Throughout the day there will be special programs to mark the occasion and a number of personages on local commercial stations will participate, including John McCaffrey, Eileen O'Connell, Pat Barnes, Mary Small, Alma Dettinger and Arlene Francis.

At 8:05 P. M. there will be a critical discussion of present-day radio, the members of the panel including the Rev. Robert I. Gannon, president of Fordham; Morris Novik, John Garrison and F. W. Carlington.

"On Your Mark," a new audience-participation item, will be added to WOR's schedule next Monday. It will be heard at 2:30 P. M. each weekday afternoon thereafter and will include prizes for questions which are correctly answered. Paul Luther will produce and announce the program.

George Shackley's original composition, "Anthem for Brotherhood," will have its first television performance at 5 P. M. Sunday over WPIX. The rendition will be a part of the station's "Television Chapel" program.

Beginning tomorrow, "Waltz Time" will be heard for a full hour for three successive Friday evenings at 9 o'clock over NBC.

A memorial tribute to Col. David Marcus, who died in action while commanding the Israeli forces on the Jerusalem front, will be presented at 10:03 this evening over WMCA. Gov. Thomas E. Dewey and Mayor O'Dwyer will be among the speakers to be heard by means of transcriptions.

Station WNEW will transmit reports on traffic conditions on the major highways in the metropolitan area for those who plan to spend the holiday week-end out of town. On Friday, the reports will be heard on the hour at frequent intervals between 4 and 11 P. M. The same schedule also will be followed on Sunday and Monday afternoons and evenings.

"The Better Half," which is to go under commercial sponsorship on Sept. 16 over the Mutual network, will take to the air as a sustainer on Aug. 19.

A device called a transistor, which has several applications in radio where a vacuum tube ordinarily is employed, was demonstrated for the first time yesterday at Bell Telephone Laboratories, 463 West Street, where it was invented.

The device was demonstrated in a radio receiver, which contained none of the conventional tubes. It also was shown in a telephone system and in a television unit controlled by a receiver on a lower floor. In each case the transistor was employed as an amplifier, although it is claimed that it also can be used as an oscillator in that it will create and send radio waves.

In the shape of a small metal cylinder about a half-inch long, the transistor contains no vacuum, grid, plate or glass envelope to keep the air away. Its action is instantaneous, there being no warm-up delay since no heat is developed as in a vacuum tube.

The working parts of the device consist solely of two fine wires that run down to a pinhead of solid semi-conductive material soldered to a metal base. The substance on the metal base amplifies the current carried to it by one wire and the other wire carries away the amplified current.

After Michael Riordan

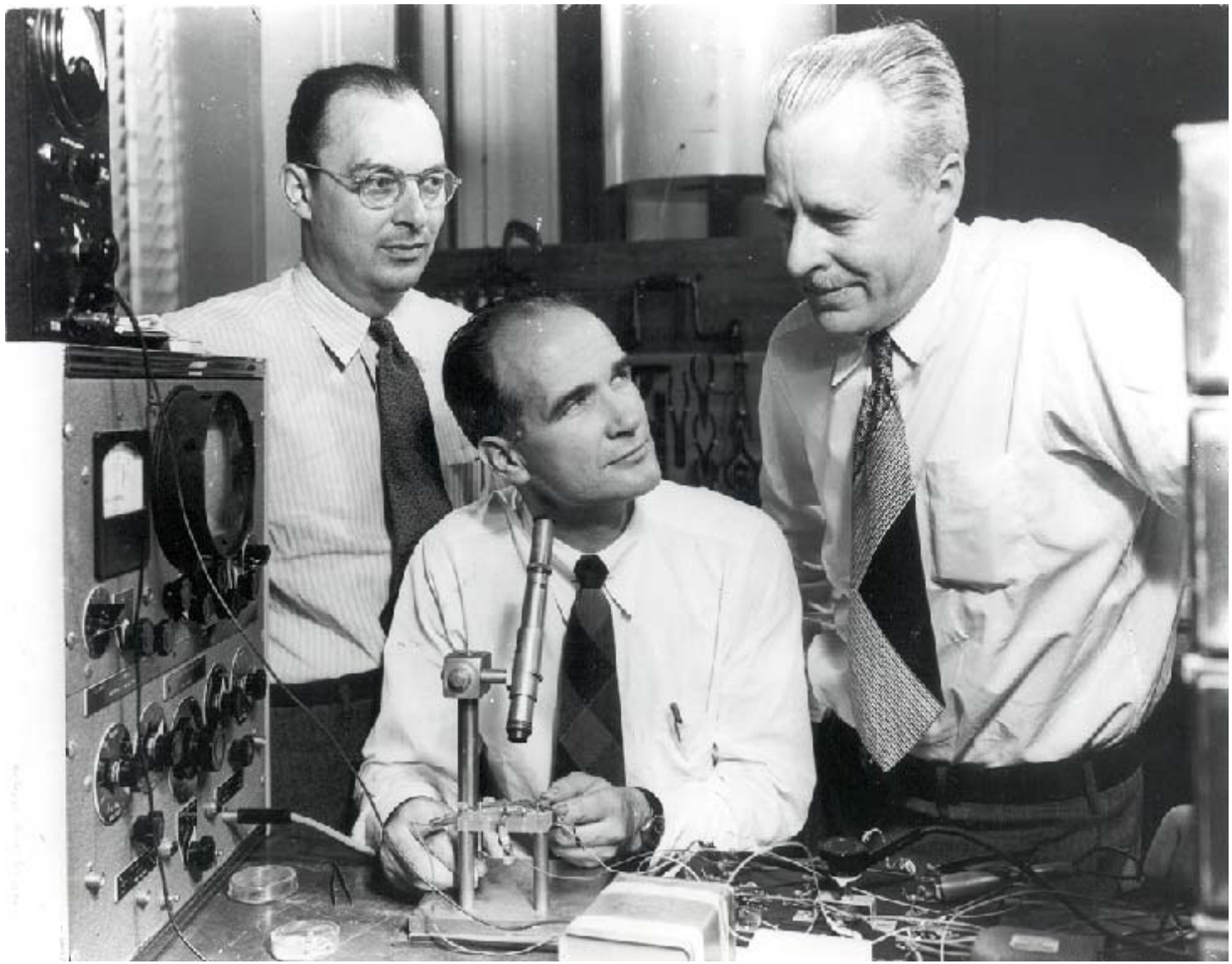
The Famous Picture

Courtesy of
Lillian Hoddeson

Brattain, Shockley and Bardeen

Courtesy of Lillian Hoddeson

The Famous Picture (25 Years Later)

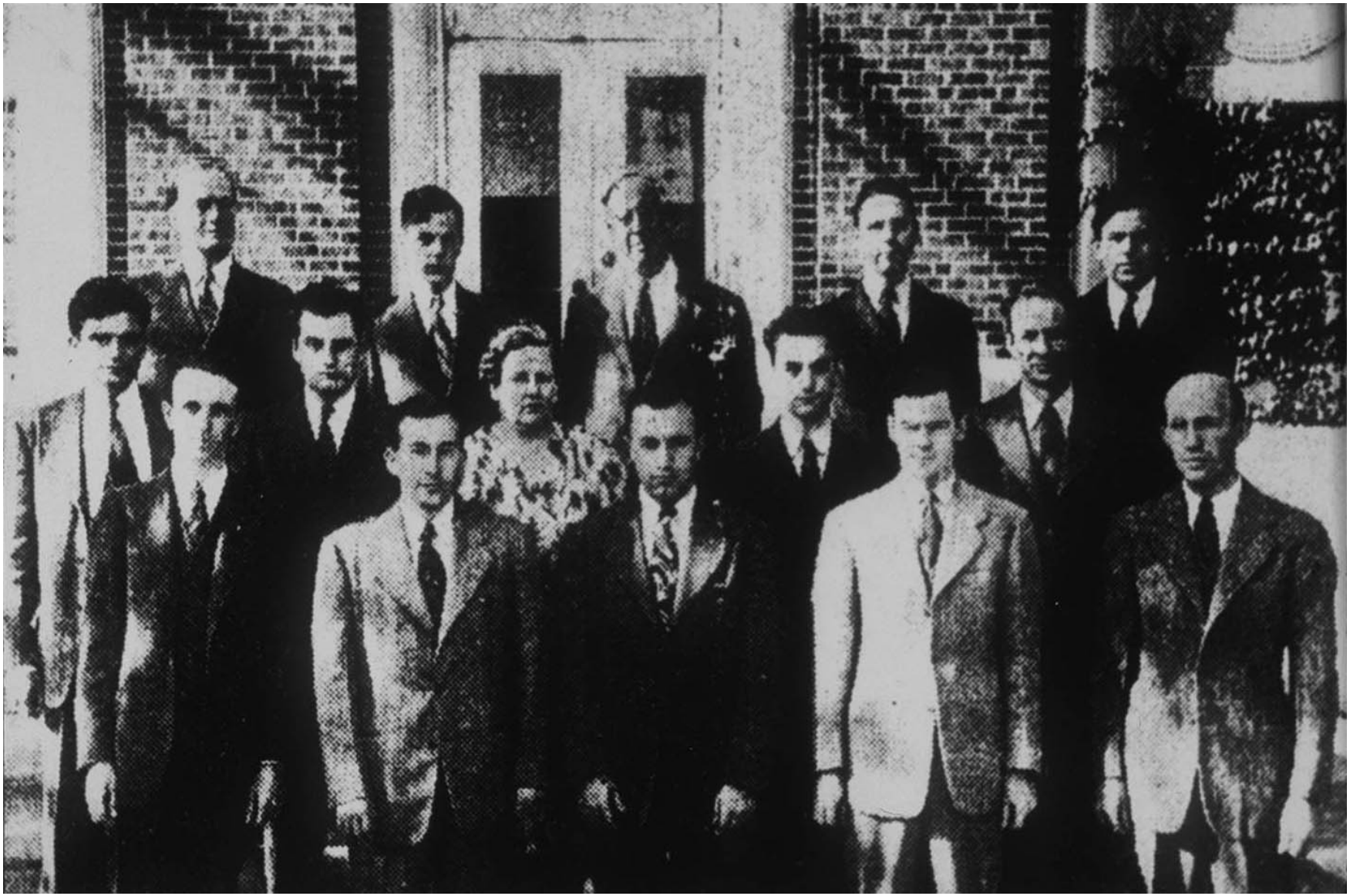


Courtesy of Lillian Hoddeson

Recapitulation - Serendipity Factors

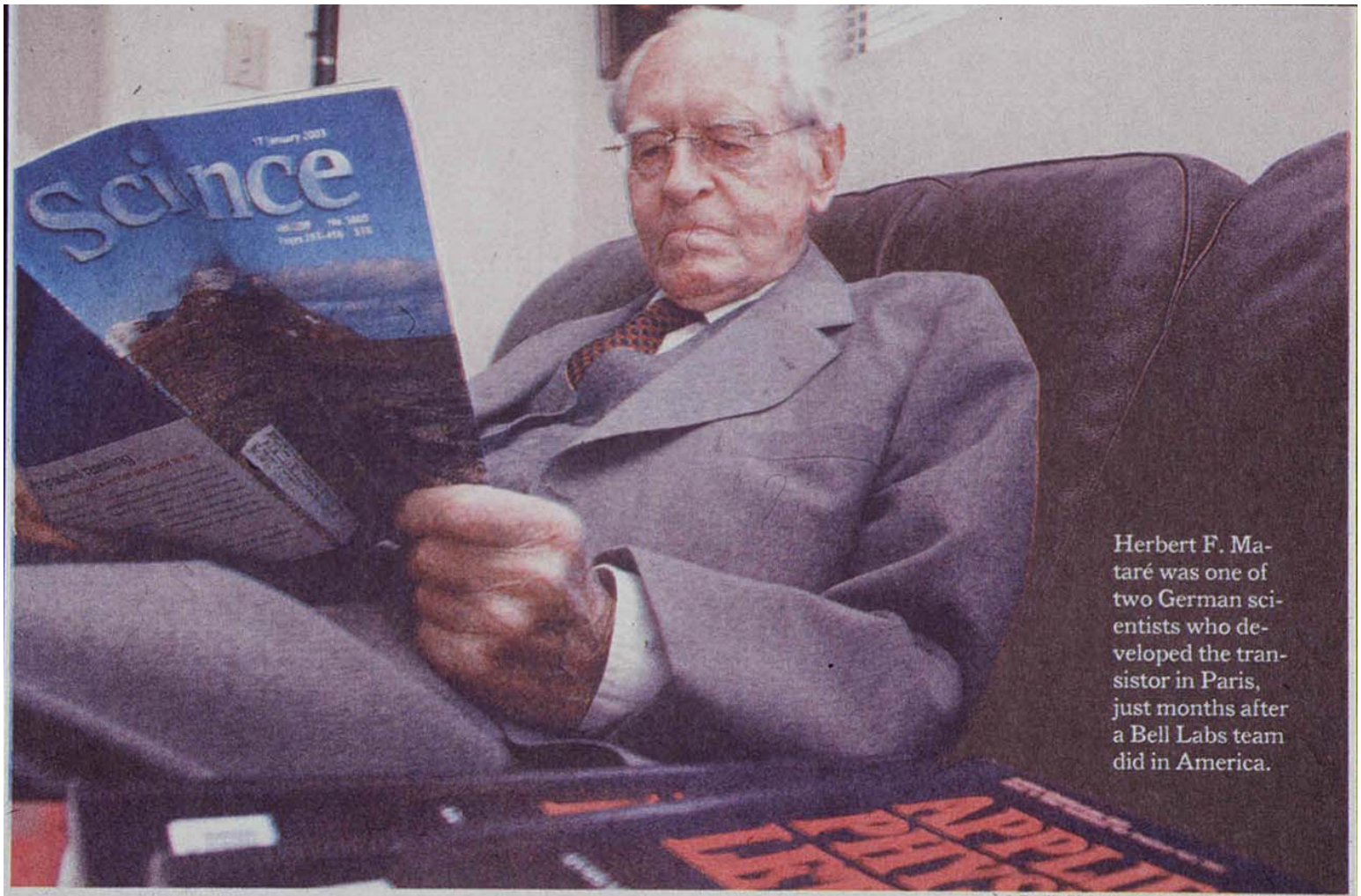
- **Solid-state amplifier invented by Bardeen and Brattain "completely different in principle and function from field-effect transistor proposed by Shockley [envisioned as majority carrier device] but served original goal as triode amplifier"**
  - **"Failure of Shockley's original field-effect transistor device"**
  - **"Bardeen's focus on surface states and inversion layer unexpectedly generated point-contact transistor configuration"**
  - **"Switch from Si to Ge"**
  - **Utilization of two whiskers "close" together**
  - **Brattain's accidental destruction (in his mind) of GeO_2 film (subsequently realized not present)**
- **"Results … obtained by admixture of accident, brilliant insight and luck …. The fact results were reverse of what they expected initially … namely that minority, rather than majority carriers, were modulated is irrelevant. Accident had favored their prepared minds! They were amply prepared to understand and exploit the breakthrough…."**
  - **"Bardeen & Brattain's attentiveness to pick up implications of their invention"**

Purdue Team



Courtesy of Fred Seitz

Herbert Matare



A Parallel Inventor of the Transistor Has His Moment

Courtesy of Fred Seitz

Patents

- Original patent application applied by BTL included Shockley's field-effect transistor, albeit effect was extremely small
- AT&T attorneys, however, found previous patents awarded for rather similar field-effect amplifiers to Lilienfeld (as early as 1930) and Heil
  - Sah has noted neither Lilienfeld nor Heil recognized necessity of inversion layer for operation of their proposed devices
- Shockley not included in point-contact patent application
- Severe disappointment became major impetus for spurring Shockley's subsequent seminal contributions
  - Injection over barrier
  - P-n junction theory
  - P-n junction transistor

J.E. Lilienfeld

Courtesy of Fred Seitz, Reprinted with permission from *Physics Today* [May 1988]:87 © 1988 American Institute of Physics.)

Summary

- **"….. Nearly all present-day field-effect transistors make use of controlling flow in an inversion layer of opposite conductivity type adjacent to surface (such as n-type inversion layer on p-type silicon.) *I [Bardeen] have basic patent on use of inversion layer to confine flow. Present-day bipolar transistors are of junction type and based on patented structure Shockley invented* while planning experiments to elucidate dynamics of point-contact transistor.**
  - **Bell Laboratories patent department was unable to obtain patent on Shockley's field-effect invention because of Lilienfeld's patents and others." *(Bardeen)***
- **"It seems likely that *many inventions unforeseen at present will be made based on the principles of carrier injection*, the field effect, the Suhl effect, *and the properties of rectifying junctions*. It is quite probable that other new physical principles will also be utilized to practical ends as the art develops." *(Shockley)***

Summary (con't)

- **"This book [Electrons and Holes in Semiconductors] had its origins in a series of lectures given at Bell Telephone Laboratories in connection with the growth of the transistor program. It thus owes its existence basically to the *invention of the transistor by J. Bardeen and W.H. Brattain*." *(Shockley)***

Summary (con't)

- **John Bardeen, co-inventor of the point-contact transistor and inventor of the MOS transistor, may rightly be called the**

father of modern electronics

Bardeen / Schottky / Brattain - Pretzfeld, 1954

After Erhard Sirtl

Agenda

- Introduction
- Threshold events
- Transistor Fabrication
  - Point-contact
  - Grown-junction
  - Alloy formation
  - Diffusion
- Mesa and planar advances
- Integrated circuit beginnings
- Bipolar DRAM IC Issues
  - (1960-1980's)
- Prognosis
- Acknowledgements

Single-Crystal Growth

- **Polycrystalline Ge and Si materials utilized at BTL and elsewhere for transistor R&D in late ’40s and early ’50s**
  - **Utilization of single crystals of Ge and Si extremely controversial**
  - **Shockley opposed work on Ge single crystals because he had publicly stated that transistor science could be elicited from small specimens of polycrystalline masses of material**
- **Teal believed criticality of single-crystals for electronics era, recognizing Shockley’s bipolar junction characteristics in single crystal Ge and Si would be substantially better and more reproducible than polycrystalline material**
- **Teal believed fundamental property of crystalline semiconductor was easily controllable and spatially variable concentration, type and mobility of free carriers**
  - **Technologically important to ensure many complex units to be identical, close performance tolerances, high yields and low cost**

Single-Crystal Growth (con't)

- **Teal reasoned essential to have high-perfection, high-purity controlled composition to achieve separation of various available electron and hole conduction processes, which was not appreciated for semiconductor applications**
  - **Required to to analyze and understand operation of devices and achieve optimum functional usage**
    - **To produce conducting medium in which a high degree of lattice perfection, of uniformity of structure and chemical purity attained**
    - **To build into this highly perfect medium in controlled way required resistivities and electrical boundaries to give a variety of device possibilities by control of chemical composition (i.e., donor and acceptor concentration) along direction of single crystal growth**

Gordon Teal

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Dopants in Silicon

- **Jack Scaff / Greiner contributed to comprehension of n- and p-type dopants in Ge and Si**
- **Dopants occupied substitutional sites in equilibrium**
- **Ground states approximately 40-50 meV from appropriate band edge in Si**

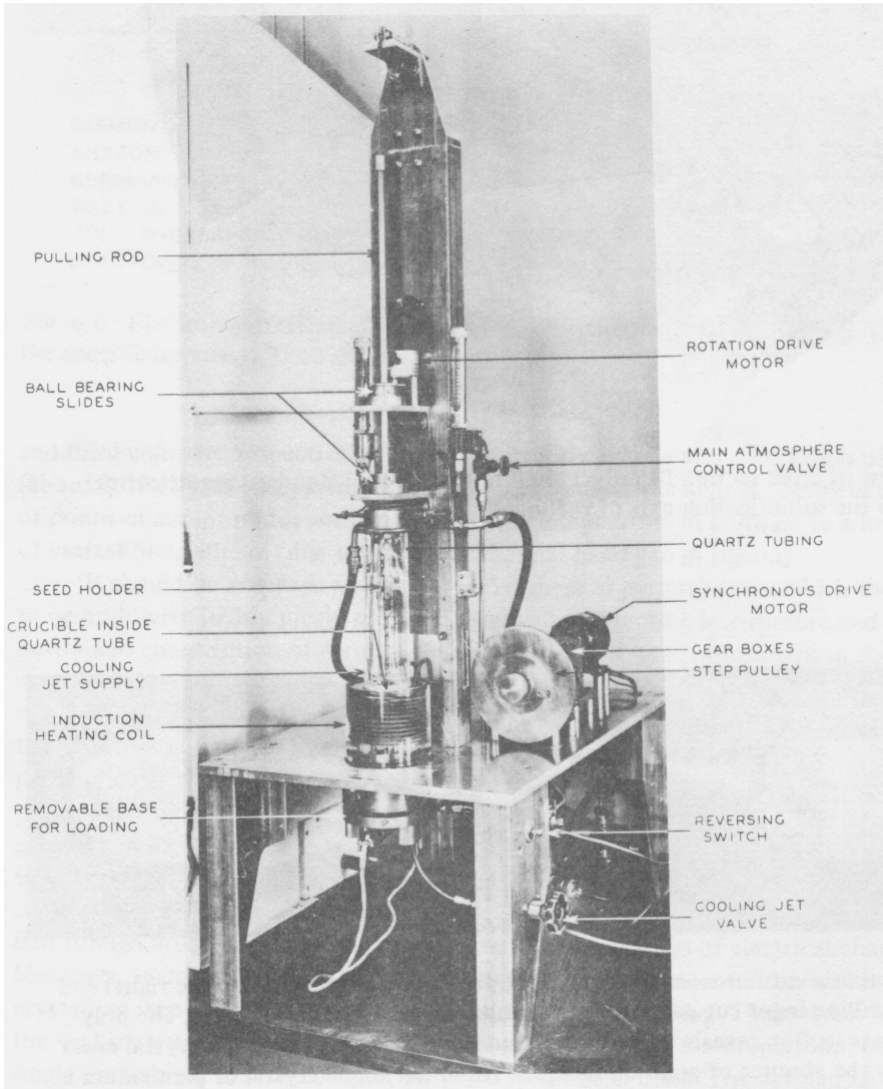
Single-Crystal Growth (con't)

- Crystalline materials facilitated experimental verification of many quantum theoretical concepts of electrons and holes
  - Effective mass
  - Drift and conductivity mobility
  - Carrier lifetime
  - Tunneling
  - P-n junction phenomena
- By early '50s all investigators of semiconductor properties & p-n junction studies of Ge/Si utilized pulled single crystals
- Teal filed p-n junction patent in single-crystal Ge in '50
- First bipolar junction transistor (n-p-n) achieved in single crystal Ge (grown-junction technique) by Shockley, Sparks and Teal in '51 – three years after discovery of transistor action by Bardeen and Brattain

Bipolar Junction Transistor (Implementation)

- ***Jun 26 '48*** **Shockley's p-n junction / p-n junction transistor theoretical analysis (*"347" patent* filed)**
- ***Apr 7 '49*** **Sparks / Mikulyak "existence proof" Ge p-n-p (non-colinear) transistor (power gain $\leq$ 16)**
- ***Jul '49*** **Shockley's extended p-n junction / p-n junction transistor theory published (Bell Syst. Tech. J.)**
- ***Apr '50*** **Teal/Buehler/Sparks single crystal research and fabrication of grown p-n junction and (double-doping) n-p-n large-area junction transistor (10-15 watts audio power $\leq$ 20 Kc)**
- ***Jan '51*** **Korean war stimulated fabrication of n-p-n microwatt junction transistor (proximity fuse)**
- ***Jul '51*** **Shockley, Sparks and Teal microwatt n-p-n junction transistor published (Phys. Rev.)**

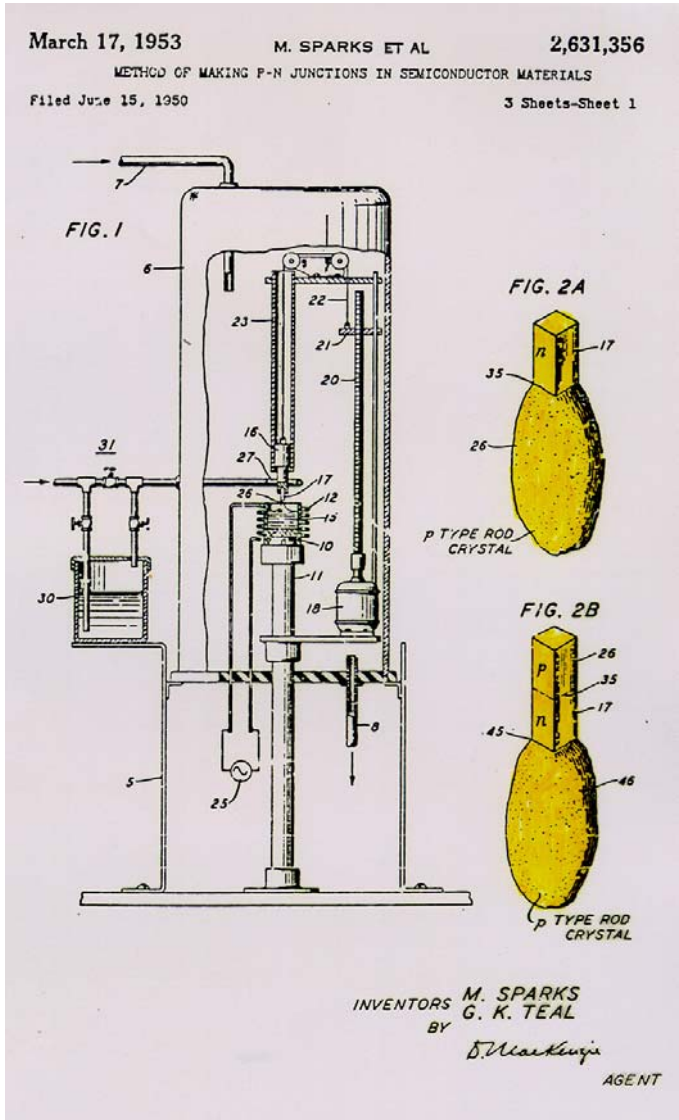
Type II Crystal-Pulling Machine Designed and Made by Teal and Little (ca 1950)



Materials and Processes: Part A: Materials, 3rd ed.,(edited by J.F. Young and R.S. Shane,1985)
Reprinted with permission of Marcel Dekker, Inc.

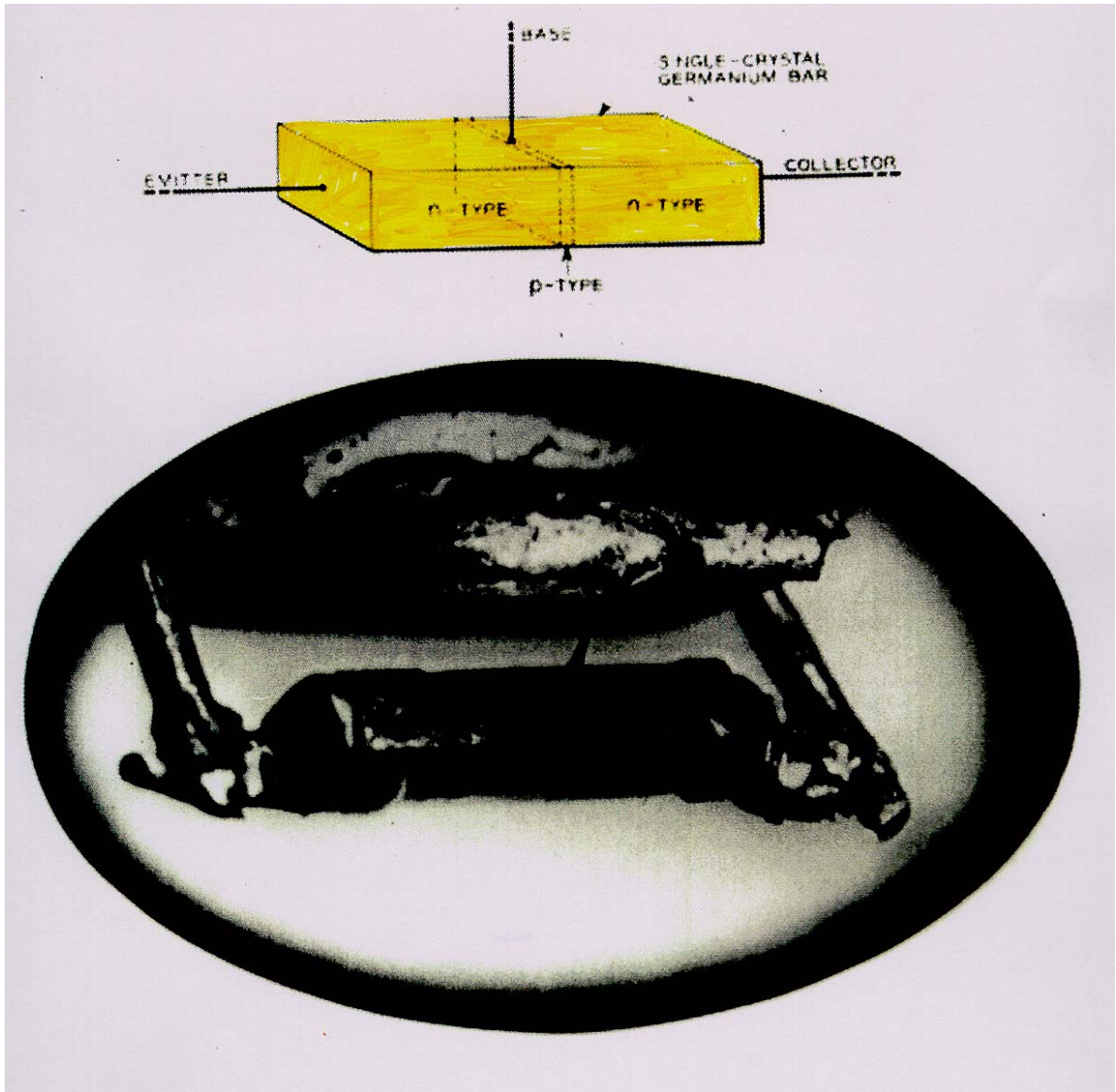
Bipolar Junction Transistor (Implementation)

Double-Doping Growth: N-P-N Large Area Junction Transistor



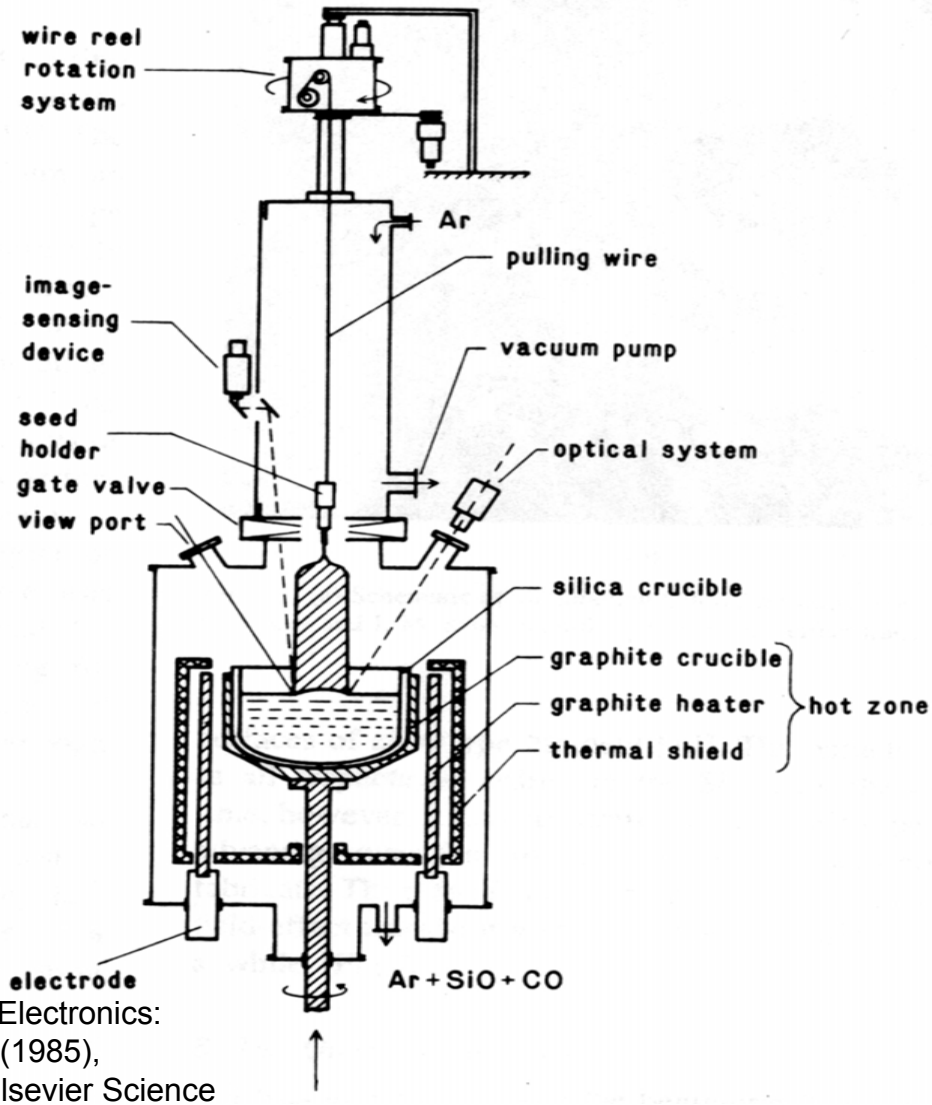
After Morgan Sparks et al. (courtesy Michael Riordan)

Bipolar Junction Transistor (Implementation)
Microwatt Junction Transistor (July 4, 1951)



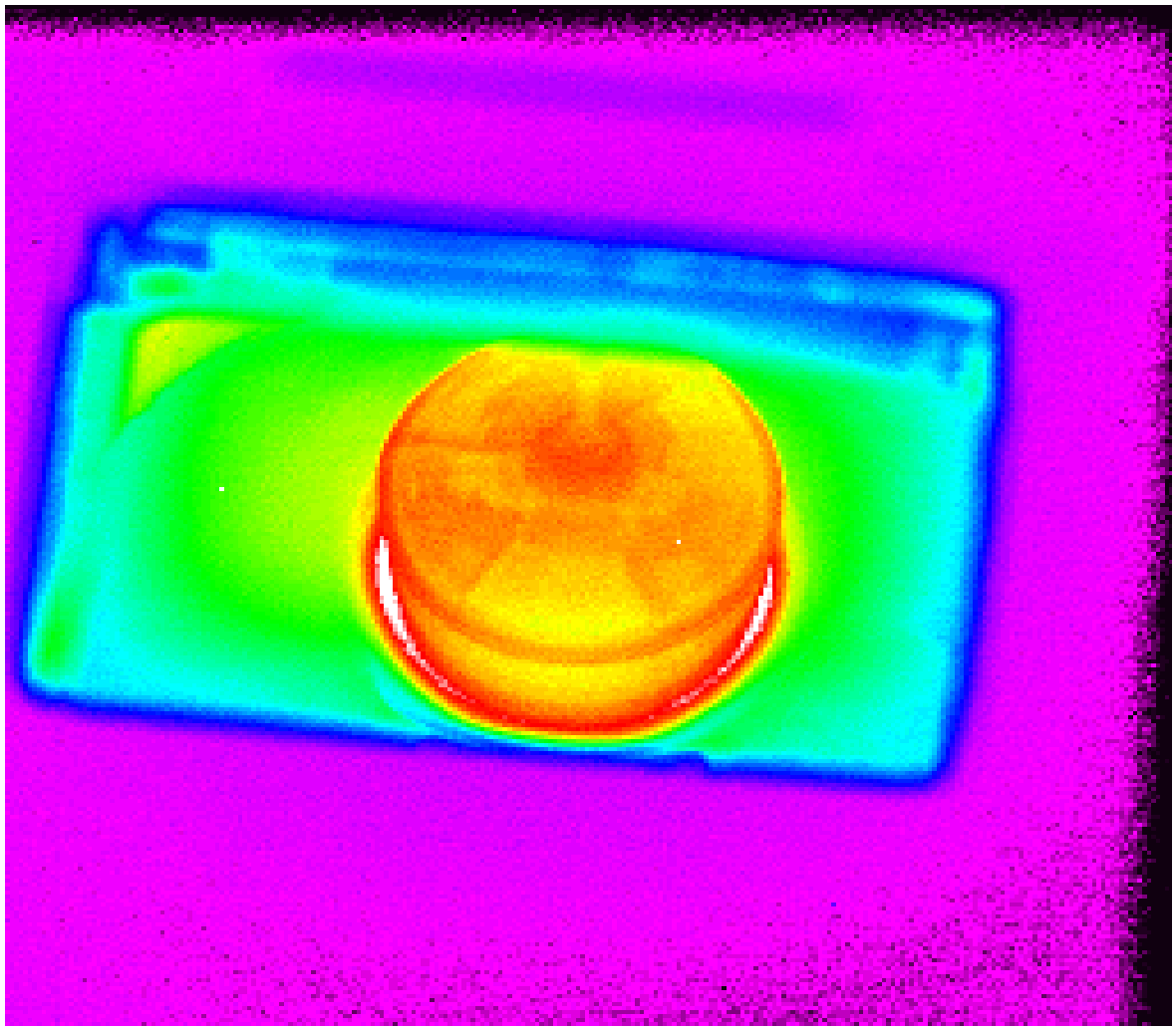
After Michael Riordan

Schematic Illustration of Typical Czochralski Puller With Hot Zone, Automatic Optical and Image Sensing Diameter Controls and Wire Reeling System



T.Abe, Crystal Fabrication, VLSI Electronics: Microstructure Science, **12**, 3-61 (1985), Reprinted with permission from Elsevier Science

Single- Crystal Pulled From Melt (150 mm Diameter, {100} Orientation)



Courtesy of Gerry Moore

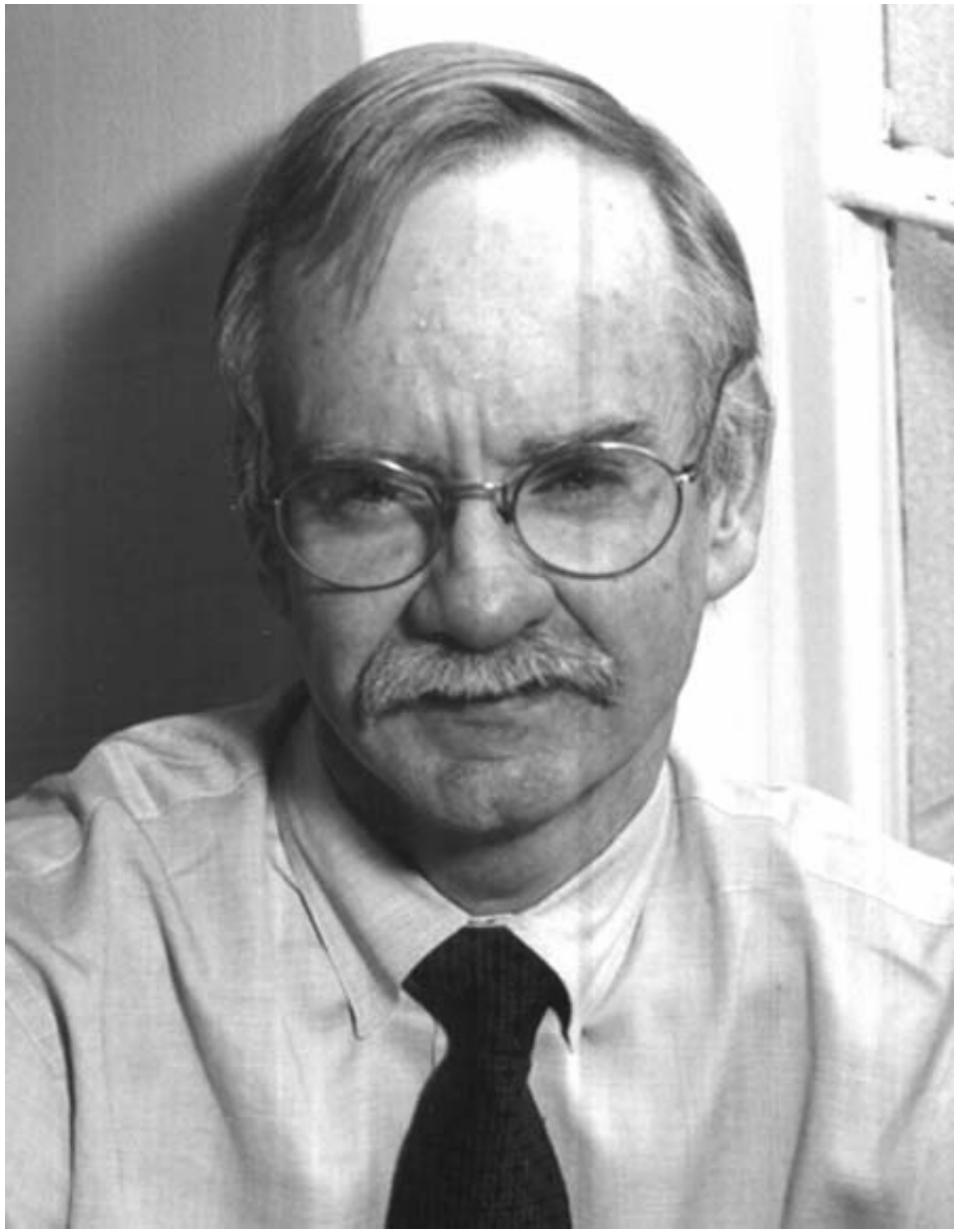
Ken Benson

Takao Abe

Wilfred von Ammon

Bob Falster (l) and Vladimir Voronkov (r)

Bob Brown



Dopant Distribution During Single-Crystal Growth

- **Normal freezing described by zone-refining technique**
  - $C_s\ (g) = k_e\ C_l\ (1\text{-}g)^{[ke\ (dl/ds)\ -\ 1]}$
    - **Bill Pfann - 1952**
  - $k_e = k_o\ [k_o + (1\text{-}k_o)\ \exp\ (-f\ \delta\ /\ D)]^{-1}$
    - **Burton-Prim-Slichter - 1953**
  - **k_o, equilibrium distribution coefficient, related to effective distribution coefficient, k_e, dependent on particulars of equipment and pulling specifics**
  - **Kenji Morizane, Gus Witt and Harry Gatos later realized the crystal growth rate, *f*, was microscopic crystal growth rate**
  - **Extensive summary of k_o and equilibrium solubilities in Ge and Si tabulated by Forrest Trumbore**

Bill Pfann

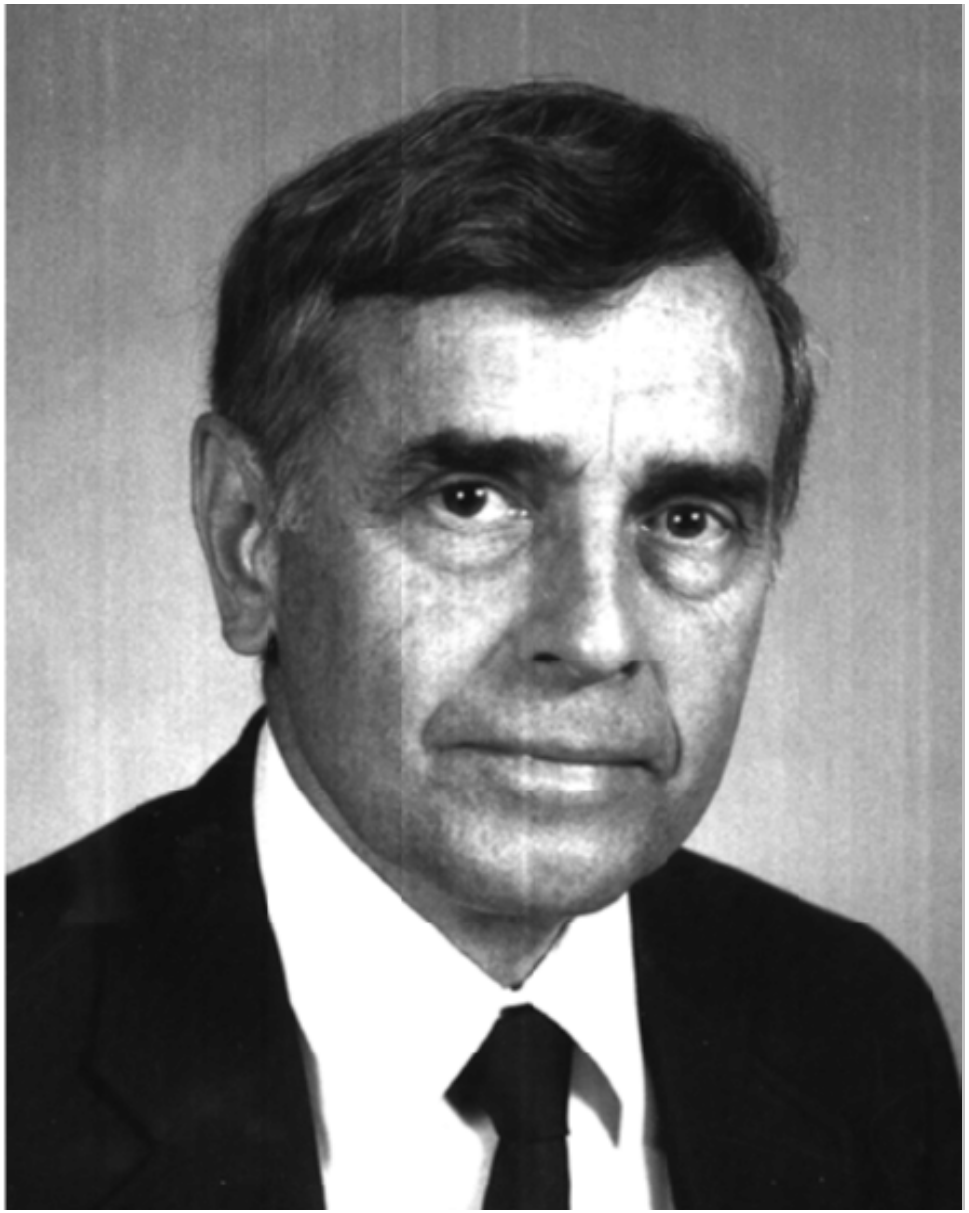
H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)

Harry Gatos (leading chamber-music quartet)

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Walt Runyan

Forrest Trumbore



H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Oxygen in Silicon

- **Innocuous observation that silicon crystals grown by Teal-Little, pulled (or inappropriately, but conventionally the CZ technique after Jan Czochralski) contains ppma concentrations of oxygen**
  - **Dissolution of quartz crucible by molten silicon**
  - **Resulted in extensive scientific literature and gettering methodologies for denuded zone formation**
  - **Optimize device performance, yield and reliability**

Bruce Hannay

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Ron Newman

Agenda

- Introduction
- Threshold events
- Transistor Fabrication
  - Point-contact
  - Grown-junction
  - Alloy formation
  - Diffusion
- Mesa and planar advances
- Integrated circuit beginnings
- Bipolar and DRAM IC Issues
  - (1960-1980's)
- Prognosis
- Acknowledgements

Double-Doping Technique (1951)

- **Pellets of Ga and Sb were sequentially (and rapidly) added to melt during growth of n-type Ge (Teal et al. - 1951)**
- **Rate-growth technique of Hall introduced in 1952 and Bridgers and Kolb - 1955**
  - **Based on variation of incorporation of acceptor or donor impurities into solidifying Ge crystal with crystal growth rate, forming both p-n junctions and n-p-n transistors**
- **Commercially grown-junction Si transistor introduced by Teal in 1954, subsequently described by Adcock in conjunction with Jones and colleagues**
  - **Experimental Si transistor previously announced in 1950 by BTL**
  - **Tannenbaum and co-workers reported in 1955 additions of Ga and Sb dopants for growth of Si crystals containing up to five n-p-n regions suitable for production of grown-junction Si transistors**

Bob Hall

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Willis Adcock

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)

Point-Contact vs Grown-Junction Transistors

- **Grown-junction Ge transistors improvements overtook point-contact transistors in early fifties**
  - **Larger current handling capability**
  - **Less junction noise**
  - **Improved techniques to control base width**
    - **Resulted in increased frequency response**
- **Eventually, Si replaced Ge**
  - **Higher temperature operation (300°C)**
  - **Lower reverse current**
  - **Increased power output**
  - **Stable oxidized surface of Si compared to Ge**
  - **Si small-area diodes replaced Ge point-contact by about 1960**
- **Si diodes first reported in 1952 by Pearson in conjunction with Sawyer and Foy via Al doped (p-type) wire alloyed to n-type Si material**

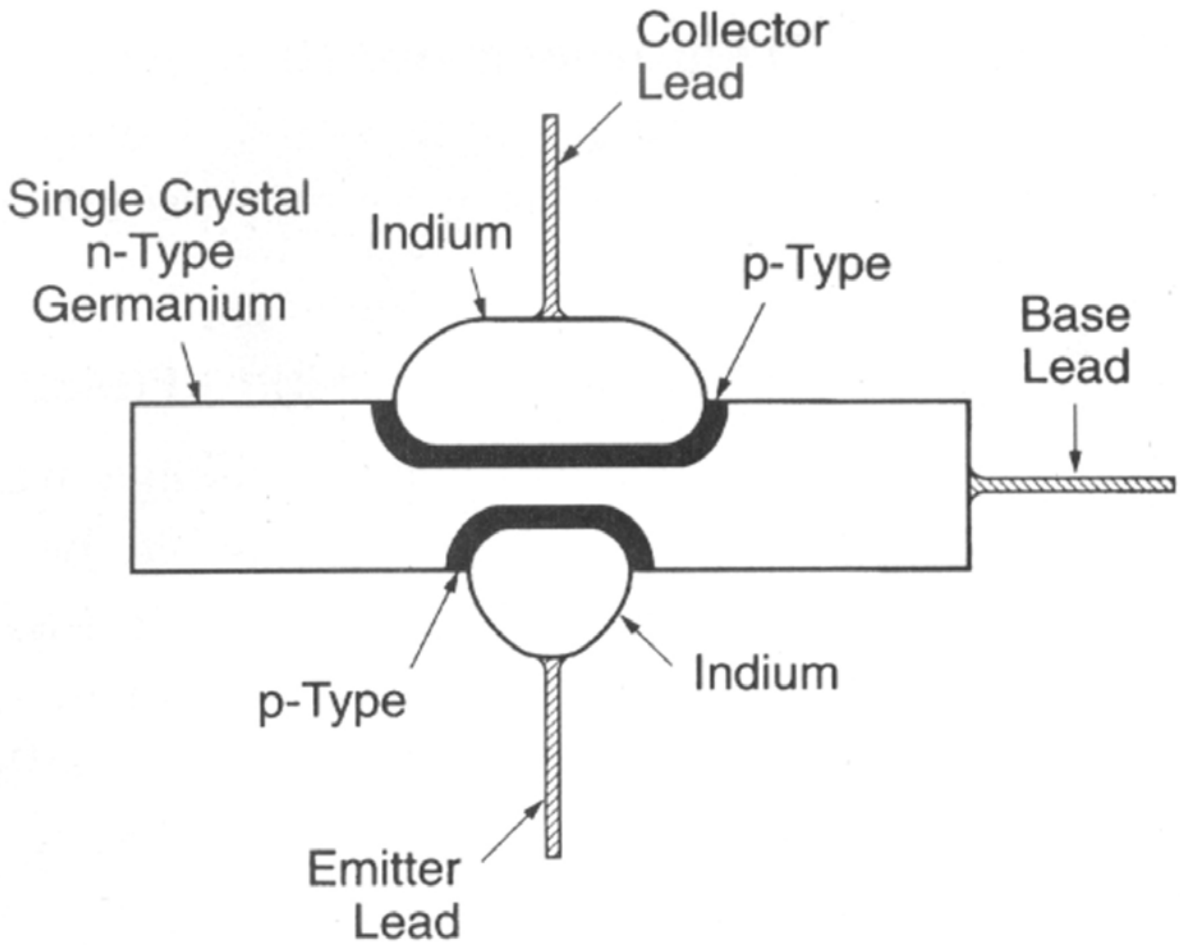
Celebrating the Point-Contact Transistor - 2000 (Gerald Pearson's 1973 Replica of 1947 Structure)

Courtesy of Jim Harris

Alloy Transistors

- **Saby developed Ge alloy transistor in 1952 as did Law and colleagues, building on Hall's research**
- **Process described, in retrospect, as crystal dissolution and regrowth at 600°C on {111} (local liquid phase epitaxy)**
  - **Recrystallized Ge incorporated In thereby converting to p-type**
  - **Achievement of precise and narrow width difficult due to precise control of temperature and diffusion from both surfaces**
  - **Maximum cut-off frequency of alloy Ge p-n-p transistor typically 10 MHz while point-contact Ge transistor typically up to 50 MHz**
  - **Nevertheless, Ge alloying (because of its presumed simplicity) readily implemented as manufacturable process and became widely utilized compared to more uncontrollable base widths for grown-junction devices for transistors in Ge and Si for many years**
  - **Si n-p-n alloy transistor quite difficult to fabricate due to process variability and never commanded significant market position**
  - **{111} surface preferred for alloy bipolar transistor gave way to {100}surface for MOS transistor in 1968 due to lower concentration of Si- SiO_2 interface states**

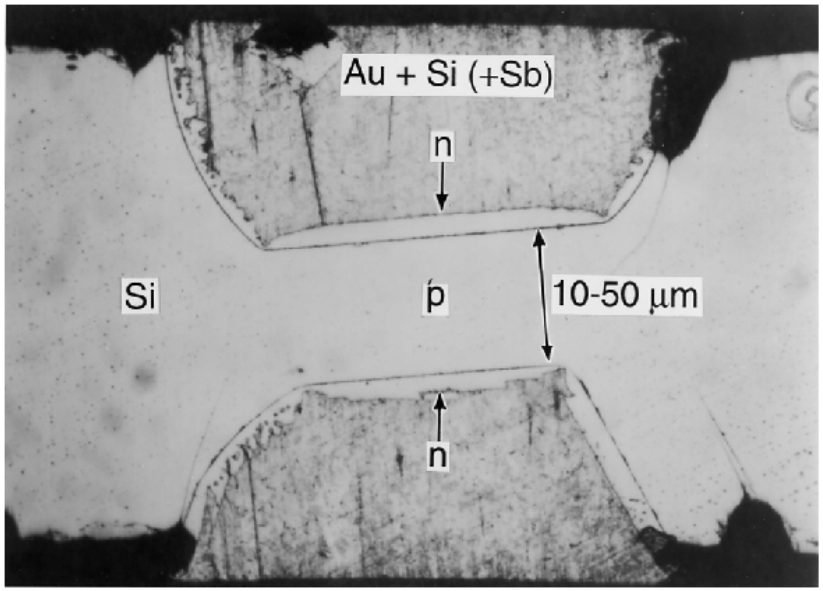
Schematic Illustration of Alloy Transistor

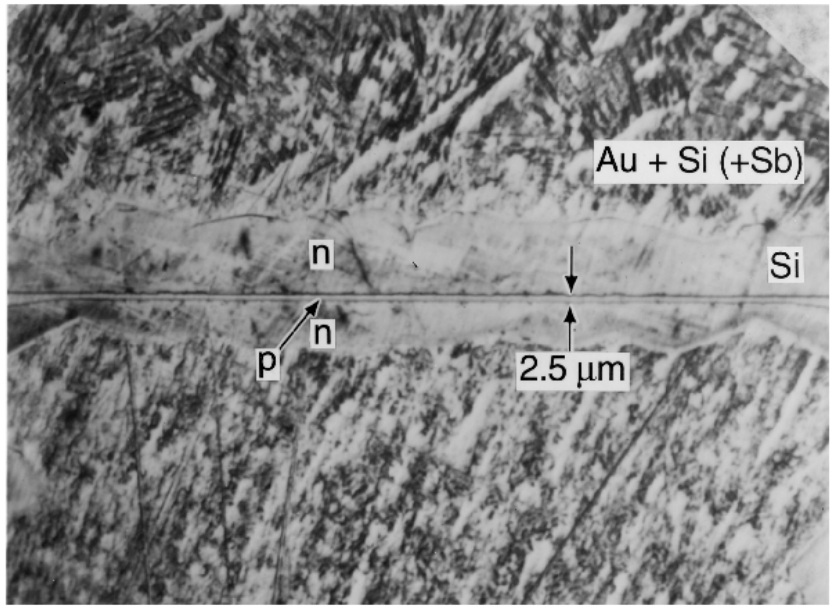


p-n–p Alloyed Germanium Junction Transistor

Ian M. Ross, *The Invention of the Transistor*, Proc. IEEE, **86**, 7-28 (1998)
Reproduced by permission of the IEEE, Inc.

Alloy Transistors





Silicon n-p-n alloyed transistor (1954) made with Au(+Sb) alloyed emitter and collector regions (D.K. Wilson, BTL, 1954). N-type emitter and collector regions regrown from Au +Si (+Sb) alloy marked with arrows. Note large base (p-type) thickness, hard to control from two sides – two references

Magnified view of alloyed n-p-n transistor showing base thickness of ≈ 2.5 μm, which, because of two reference surfaces (top and bottom and thick crystal and thick alloy) is difficult to achieve and to reproduce.

N. Holonyak, ULSI Process Integration III, ECS **PV 2003-06** (2003)

Alloy Transistors (con't)

- Alloy junctions exhibit abrupt emitter-base step junction while grown-junction are graded
  - Ge alloy transistors thereby exhibited higher alpha cut-off frequency (f_c) range (5-10 MHz) compared to grown-junction transistors (1-10 MHz)
- Abrupt base-collector junction for alloy transistor, however, resulted in higher capacitance per unit area, tending to limit high-frequency response
- Although point-contact Ge transistor $f_c \Rightarrow$ 50 MHz, grown-junction and alloy-junction devices dominated mass production into late 1950's

Diffused Bipolar Transistors

- Double-doping and rate-growth crystal techniques critical to proving out junction transistor theory
  - Junctions physically inside crystal and p-type base layer thicker and less uniform than desired
- Solid-state diffusion ($\sqrt{Dt}$) patent filed by Theurerer in 1951
  - Implemented in 1954 by Pearson and Fuller
  - In-diffusion of impurities in controlled ambient over whole semiconductor wafer ($\approx$ 1 inch diameter)
- Fuller described donors and acceptors in Ge (1952) and Fuller and Ditzenberger – donors and acceptors in Si (1954)
- Solid-state-diffusion processes fabricated in mesa structure for n-p-n and p-n-p transistors in mid-1950's
- Tannenbaum and Thomas utilized simultaneous diffusion of both acceptor (base) and donor (emitter) in fabrication of Si transistor in 1956

Diffusion Issues

- Advent of diffusion process transferred f_c limitation from base to collector
- Higher collector resistivity, compared to emitter and base, led to significant collector series resistance, coupled with collector capacitance, limited frequency response
- Reduced collector resistivity increased base-junction capacitance and lowered breakdown voltage inasmuch as base resistivity also decreased to reduce base resistance
  - Small base width required to reduce transit time
- Early's concept of p-n-i-p design modification suggested f_c values as high as 3 GHz, with experimental values of 95 MHz realized, although diffusion from both surfaces resurrected control of base width
- Early also introduced concept of heavily-doped thin base such that portion of reversed base-collector space charge penetrated into base, thereby reducing transistor transit time

Epitaxial Fabrication

- **Solution to p-n-i-p or n-p-i-n structure obtained by fabrication of lightly doped layer of silicon on heavily doped silicon substrate (epitaxial fabrication)**
- **Theurerer and colleagues (1960) expanded Murphy's localized, high-concentration sub-collector diffusion in lightly doped Si substrate**

Ken Bean

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Technology Evolution For Controlled Base Width Transistors

Technology	Author	Approximate Year	Reference
Double-doping	Teal	1951	64
Rate-grown	Hall	1952	123-125
Alloy	Hall	1950	138,139
Electrochemical thinned base	Tiley and Williams	1953	146
Diffused base	Pearson and Fuller	1954	150
P-N-I-P (N-P-I-N)	Early	1954	163
Planar process	Hoerni	1960	12
Epitaxy	Teal,Sangster, Mark, Theuerer	1954, 1957-1960	166-169

Agenda

- Introduction
- Threshold events
- Transistor Fabrication
  - Point-contact
  - Grown-junction
  - Alloy formation
  - Diffusion
- Mesa and planar advances
- Integrated circuit beginnings
- Bipolar and DRAM IC Issues
  - (1960-1980's)
- Prognosis
- Acknowledgements

Frosch and Derrick

- **Holonyak's work on diffused-base alloyed emitter p-n-p transistors and p-n-p-n thryistors required redistribution "drive-in" of donor impurity typically in H_2 at $\geq 1100°C$**
  - **Wafer surface would invariably be eroded, pitted or destroyed but a colored oxide was observed by Frosch - Spring, 1955**
- **Holonyak converted Frosch diffused Si n-p-n into working p-n-p-n thryistor**

Frosch and Derrick (con't)

- **Frosch and Derrick switched from dry-gas (typically N_2 or H_2) impurity diffusion ambient to wet ambient (H_2) vapor + carrier gas) diffusion due to exhaust H_2 igniting and flashing-back into diffusion chamber (because of gas flow fluctuations), causing H_20 to cover, react with and protect Si wafer with oxide**
- **Wet ambient created a protective oxide on Si, which could be selectively removed for gaseous diffusion into bare regions, which could then be resealed with oxide for higher temperature anneals of further diffusion**
  - **Only Ga was found to penetrate SiO_2 protective oxide**
- **Process so flexible that planar n-type regions of any desired pattern could be prepared on p-type substrate (or vice-versa)**
- **All other procedures were immediately rendered obsolete**

Frosch and Derrick (con't)

- **Frosch noted**
  - **"In addition to possibilities of process simplification, protective quartz envelope added during heating may be useful for protecting an electrical device from atmospheric conditions**
  - **Device might prove more stable if left enclosed in such a quartz envelope**
  - **However, may not be possible to make all necessary electrical contacts through quartz**
  - **Some protection may be retained by removal of small area of envelope for application of contacts**

N. Holonyak, ULSI Process Integration III, ECS **PV 2003-06** (2003);
C.J. Frosch and L. Derick, BTL Memorandum #55-113-23 (June 14, 1955)

Calvin Frosch

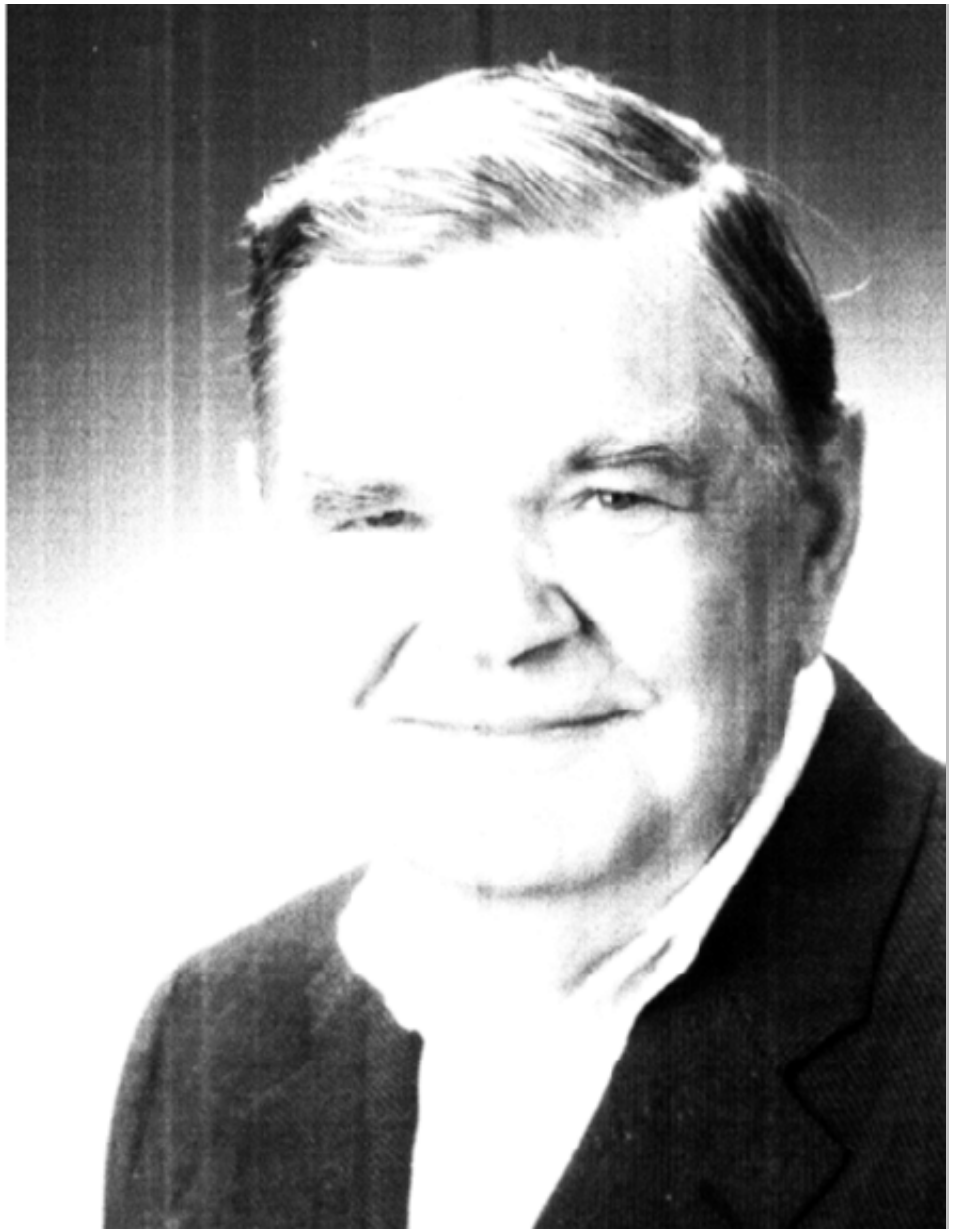
Courtesy of Nick Holonyak

Moll and Holonyak at BTL (1954-1955)

- **Moll and Holonyak now had available all critical elements for fabrication of Si transistors**
  - **Oxidation**
  - **Diffusion**
  - **Photolithography**
  - **Aluminum metallization**
  - **Thermocompression bonding**

N. Holonyak, ULSI Process Integration III, ECS **PV 2003-06** (2003);

John Moll



Nick Holonyak

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Nick Holonyak and John Bardeen

Courtesy of Lillian Hoddeson

Bardeen, Kikuchi and Holonyak
An Enduring Friendship

Courtesy of Lillian Hoddeson

Silicon – Silicon Dioxide Interface

- **Holonyak noted "remove the oxide, say it doesn't exist, and then what would there be? Silicon itself is, of course, the critical ingredient followed by its unique natural oxide. In some sense it could be said that Si and its technology (its oxide) "invented" the IC"**

Nick Holonyak, ULSI Process Integration III, ECS **PV 2003-06** (2003)

Silicon – Silicon Dioxide Interface

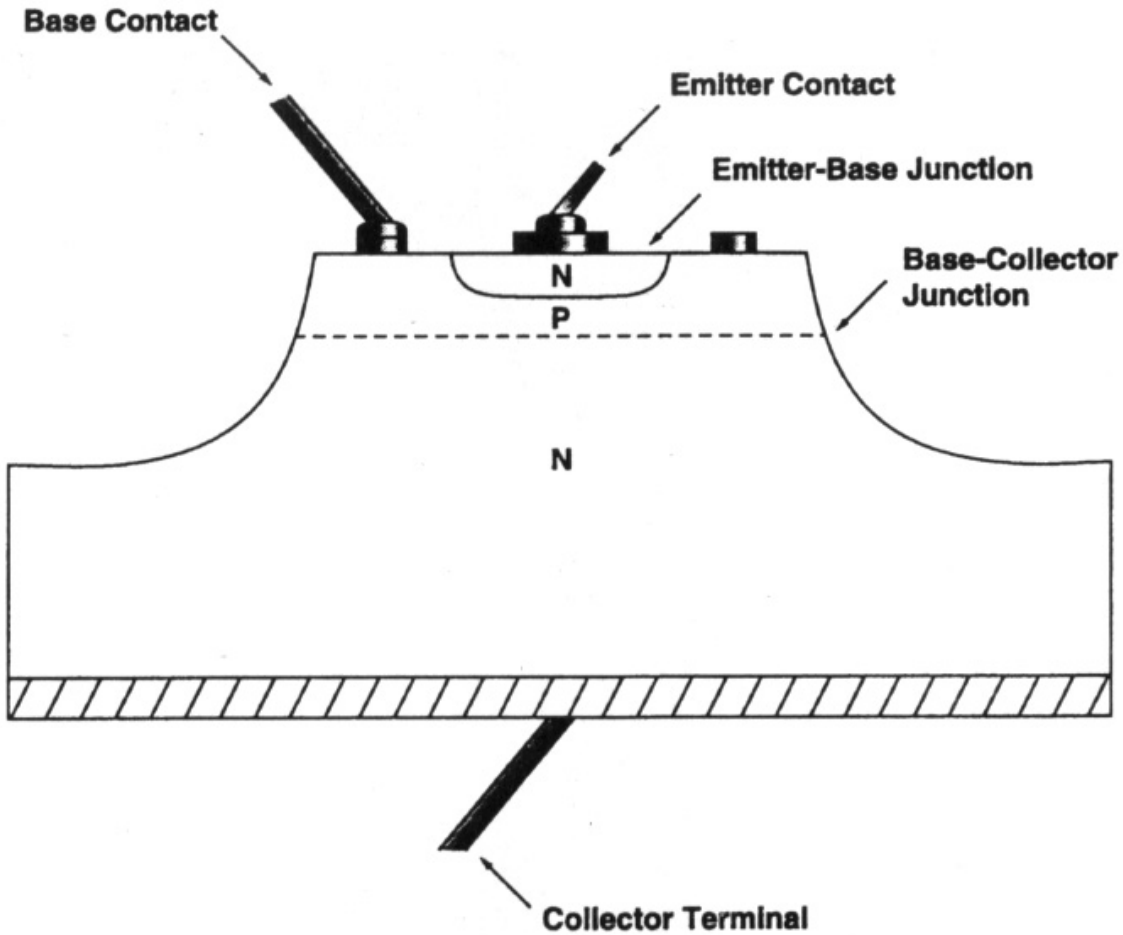
- **Si-SiO_2 diffusion technology, transferred from AT&T's Bell Telephone Laboratories (BTL) to Shockley Semiconductor and, therefore, to Fairchild Semiconductor Corporation led to phenomenon of "Silicon Valley" and creation of the IC industry**

Nick Holonyak, ULSI Process Integration III, ECS **PV 2003-06** (2003)

Fairchild Semiconductor Corporation

- **Shockley Semiconductor's original goal (1955) was fabrication of double-diffused transistors before Shockley re-directed effort to p-n-p-n diodes**
- **Blank, Grinich, Hoerni, Kleiner, Last, Noyce, Moore and Roberts departed in 1958 from Shockley Semiconductor and formed Fairchild with goal of**
  - **Fabrication of double-diffused transistors for commercial gain**
  - **Major stimulus to invention of planar transistor, Silicon Valley and development of fledgling electronics industry**

Schematic Cross-Section of Early Mesa Transistor Made by Fairchild Semiconductor Corporation



G.E. Moore, *The Role of Fairchild in Silicon Technology in the Early Days of "Silicon Valley,"* Proc. IEEE, **86**, 53-62 (1998) Reproduced by permission of the IEEE, Inc.

Mesa Transistor

- **Utilized dopant diffusion with Frosch and Derrick's oxide masking and photolithographic technique**
  - **Removal of portion of top of semiconductor wafer – mesa structure – reduced p-n junction area and depletion capacitance and achieved desired f_c**
  - **Device fabrication at planar surface with several tenths μm base widths and increased f_c**
  - **Many devices fabricated on Ge or Si wafer concurrently with rather similar characteristics**
  - **Less expensive to fabricate mesa transistor compared to grown-junction or alloy transistors**
    - **Cumulative process experience (i.e., learning curve) Haggerty**
- **All methods prone to excessive leakage currents**

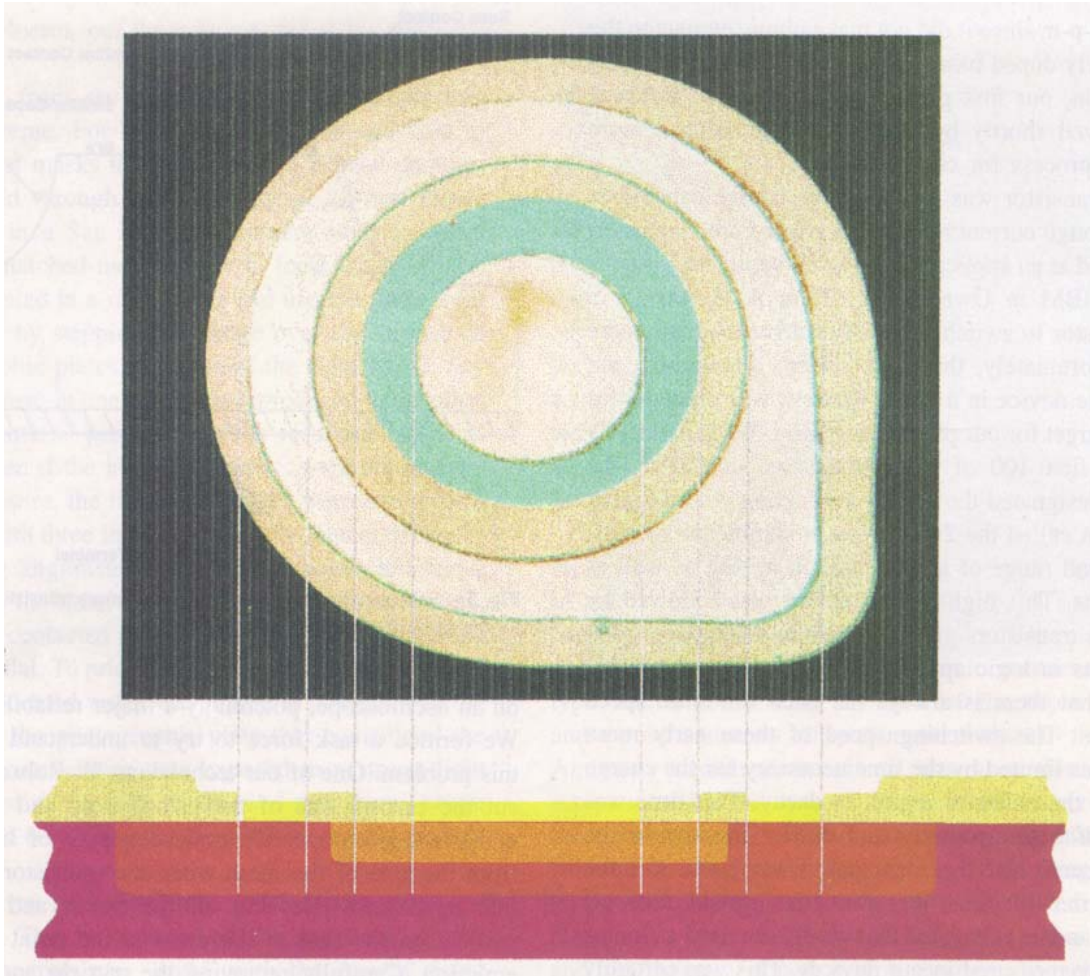
Jean Hoerni / Fairchild

- Attala and colleagues (1959) showed that SiO_2 grown under clean and controlled conditions, on properly cleaned Si wafer, would lead to reduction of surface states and passivation of Si surface
- Hoerni pulled all strands together for fabrication of planar Si transistors and diodes (1960)
  - SiO_2 masking layer utilized for
    - Fabrication of diffused Si transistors
    - Left in place for passivation of p-n junctions intersecting surface for grown-junction, alloy and diffused mesa transistors, without necessity of growing passivating oxide under meticulously clean conditions
    - Ensured dielectric layer for supporting metallic conductor overlayers in IC era

Silicon Dioxide: Prototypical Gate Dielectric

- **Passivates** silicon surface and p-n junctions intersecting surface
  - $D_{it} \approx 1 - 3 \times 10^{10}$ $(eV\text{-}cm^2)^{-1}$
- **Patternable mask** for localized diffusion of commonly utilized dopants in silicon for p-n junction fabrication
  - Amorphous, blocking layer
- **Insulator** (9 eV)
  - Affords convenient material for deposition of **adherent**, conducting films connecting various device components, separating metallic conductor films from silicon

Photomicrograph of First Planar Transistor

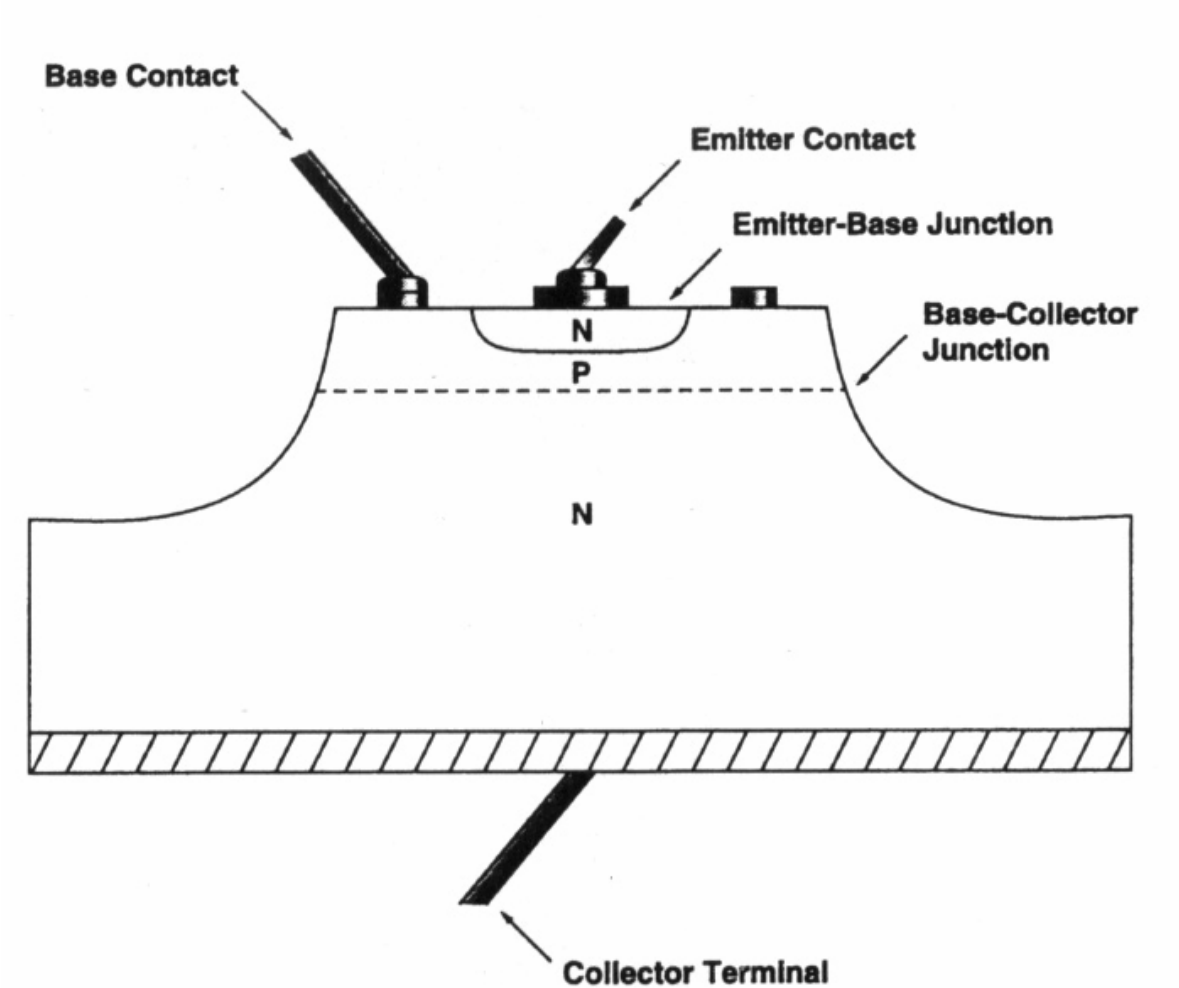


- **Diameter of circle forming most of outside ring is 0.030 in. Light areas are aluminum emitter and base electrodes.**

(From "A Solid State of Progress," Fairchild Camera and Instrument Corporation, 1979)

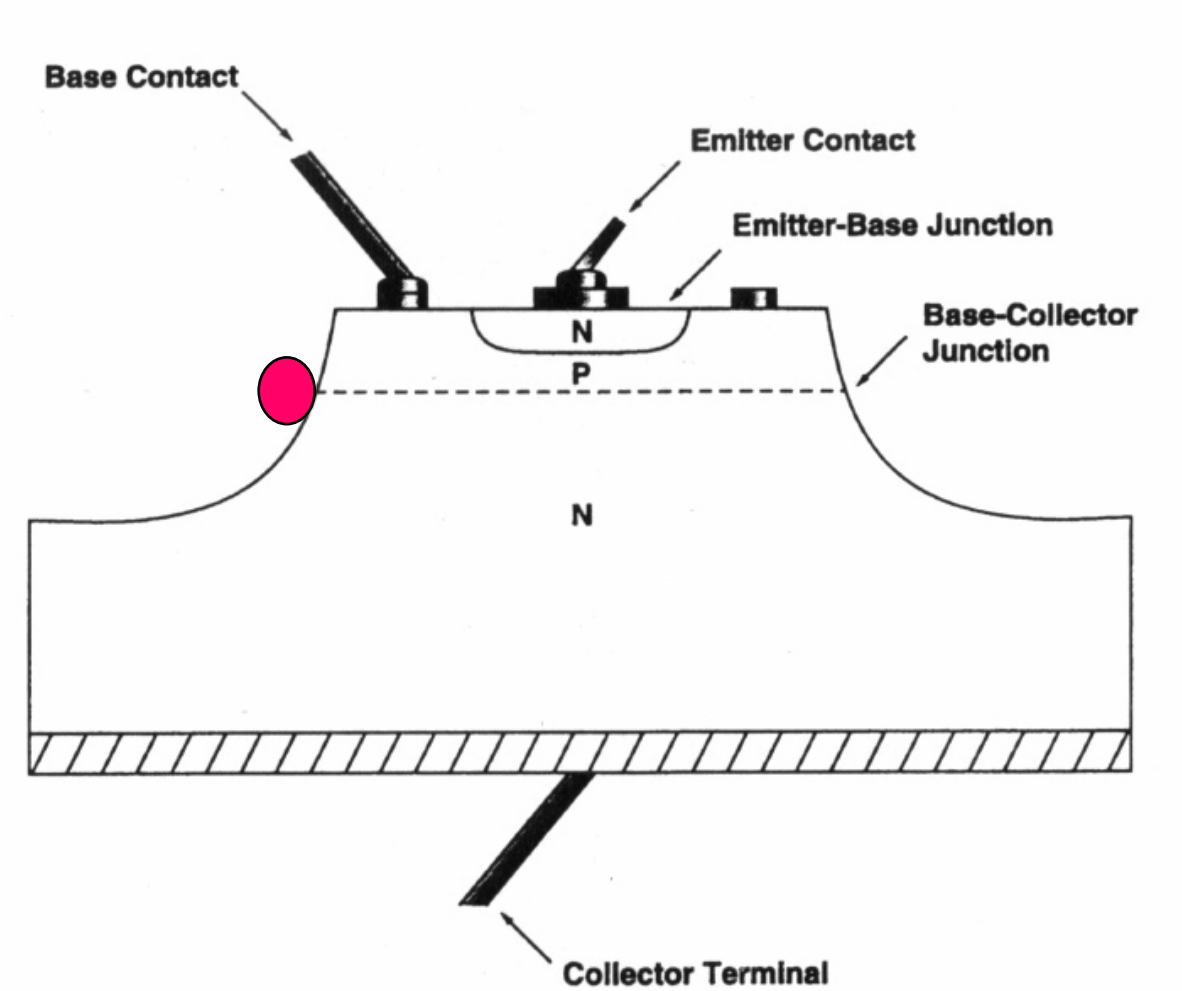
G.E. Moore, *The Role of Fairchild in Silicon Technology in the Early Days of "Silicon Valley,"* Proc. IEEE, **86**, 53-62 (1998) Reproduced by permission of the IEEE, Inc.

Schematic Cross-Section of Early Mesa Transistor Made by Fairchild Semiconductor Corporation



G.E. Moore, *The Role of Fairchild in Silicon Technology in the Early Days of "Silicon Valley,"* Proc. IEEE, **86**, 53-62 (1998) Reproduced by permission of the IEEE, Inc.

Schematic Cross-Section of Early Mesa Transistor Made by Fairchild Semiconductor Corporation



Adapted from G.E. Moore, *The Role of Fairchild in Silicon Technology in the Early Days of "Silicon Valley,"* Proc. IEEE, **86**, 53-62 (1998)

Jean Hoerni / Fairchild (con't)

- Moore noted mesa transistor configuration
  - Regions of high electric field where junction comes to surface sensitive to contamination
  - Emitter-base junction exposed on top surface between metal contacts decreases transistor gain
  - Base-collector junction intersects mesa sides,decreases breakdown voltage and modifies leakage characteristic
- Source of low breakdown voltage correlated to localized light emission from side of mesa
  - Particle observed on mesa side where light originated
    - Particle believed attracted to region's high electric field where junction intersected surface, inducing premature junction breakdown
  - Removal of particle restored device characteristics

Jean Hoerni / Fairchild (con't)

- **Planar process introduced extreme flexibility in fabrication of junction transistors**
  - **"Tooling up" to fabricate different devices involved changing mask set, diffusion profiles and doping levels in conjunction with starting Si wafer's resistivity**
- **Planar process facilitated fabrication of double-diffused transistor essentially planar with original wafer surface, without necessity of mesa structure**
- **Cut-off frequences of 10 GHz achieved, $\Rightarrow$ values for vacuum tubes**

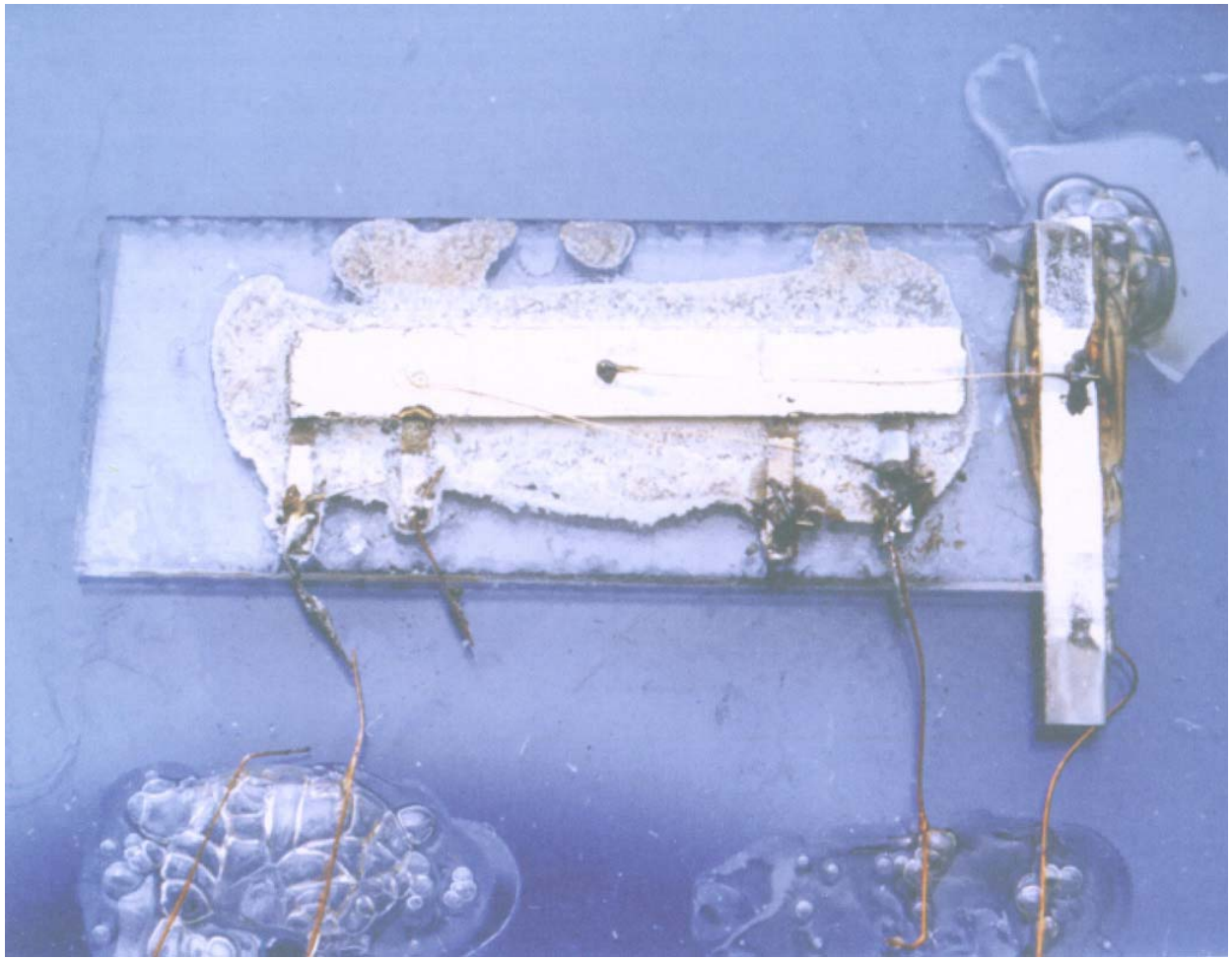
Modern Silicon MOSFETs

- *1955*: Ross's patent utilized ferroelectric as gate dielectric
- *1957*: Wallmark FET patent
- *1959*: Weimer thin-film FET utilized CdS as gate dielectric
- *1959*: Atalla et al. proposal of thermally grown SiO_2 as gate dielectric and stabilization of silicon surface
- *1960*: Ligenza and Spitzer proposal of high-pressure steam oxidation of silicon
- *1960*: Kahng and Atalla's description of NMOSFET in patents / literature
- *1963*: Hofstein and Heiman's (MOSFET) IGFET

Agenda

- Introduction
- Threshold events
- Transistor Fabrication
  - Point-contact
  - Grown-junction
  - Alloy formation
  - Diffusion
- Mesa and planar advances
- Integrated circuit beginnings
- Bipolar and DRAM IC Issues
  - (1960-1980's)
- Prognosis
- Acknowledgements

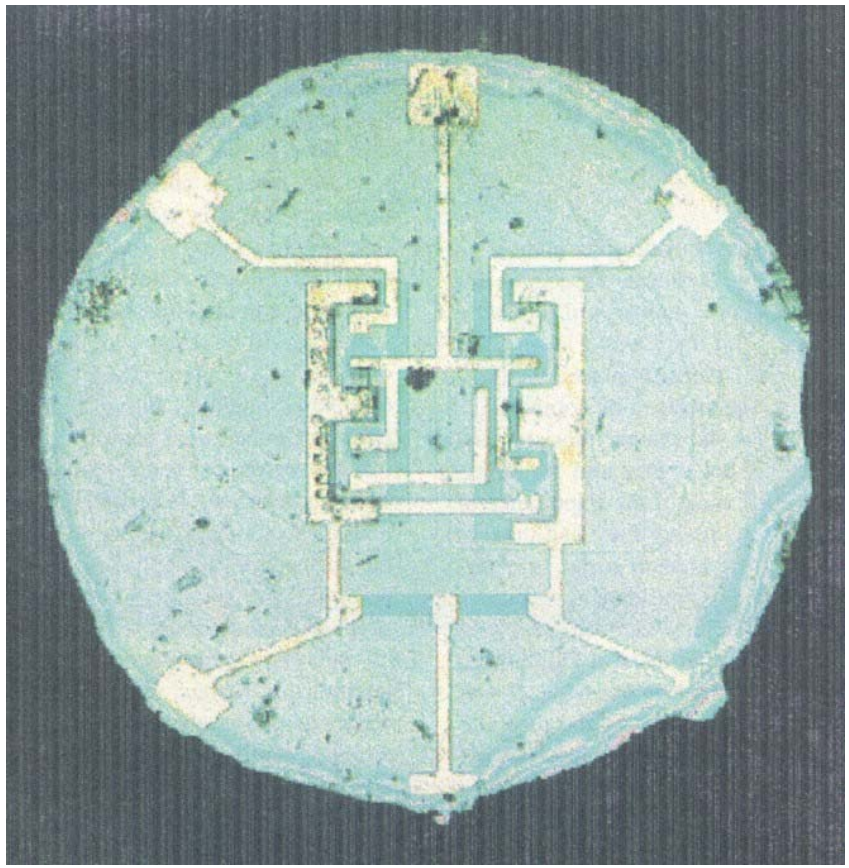
First Integrated Circuit, a Phase Shift Oscillator Fabricated in Ge, Using Mesa Process, Invented by Jack S. Kilby of Texas Instruments in 1958



Courtesy of Texas Instruments, Inc.

Jack Kilby

Photomicrograph of One of First Planar Integrated Circuits Fabricated in Si at Fairchild in 1959



Some of the aluminum interconnection metal has been damaged during etching operations to form a circular chip of silicon to plane into a transistor can modified to have more leads. (From "A Solid State of Progress," Fairchild Camera and Instrument Corporation, 1979)

G.E. Moore, *The Role of Fairchild in Silicon Technology in the Early Days of "Silicon Valley,"* Proc. IEEE, **86**, 53-62 (1998) Reproduced by permission of the IEEE, Inc.

Bob Noyce

Courtesy of Intel Corporation

Integrated Circuit Beginnings

- **Critical difference between two patents (i.e., interconnection of elements) clarified by Runyan and Bean**
- **Kilby noted "… electrically conducting material such as gold may then be *laid down* (italics entered by author) on the insulating material to make the necessary electrical connections"**
- **Noyce noted "… an electrical connection to one of said contacts comprising a conductor *adherent to said layer* (italics entered by author)…"**
- **Disagreement centered around whether "laid down" was equivalent to "adherent to"**

Integrated Circuit Beginnings (con't)

- Probably most balanced assessment of Kilby's and Noyce's relative contributions is contained in citations of Franklin Institute's 1966 Ballantine Medal award, which Kilby and Noyce shared (Runyan and Bean)
- Kilby credited for "conceiving and constructing the first working monolithic circuit in 1958," and Noyce for 'his sophistication of the monolithic circuit for more specialized use, particularly in industry" (Runyan and Bean)
- Kilby noted great strength of IC concept was it drawed on mainstream efforts in progress for semiconductor industry
  - Because of commonality with existing processes, ICs rapidly moved into production status
- MOSFET IC revolution really exploded in 1973 when IBM chose n-channel Si MOSFET instead of slower p-channel for mainframe memory computer (IBM-370/158)

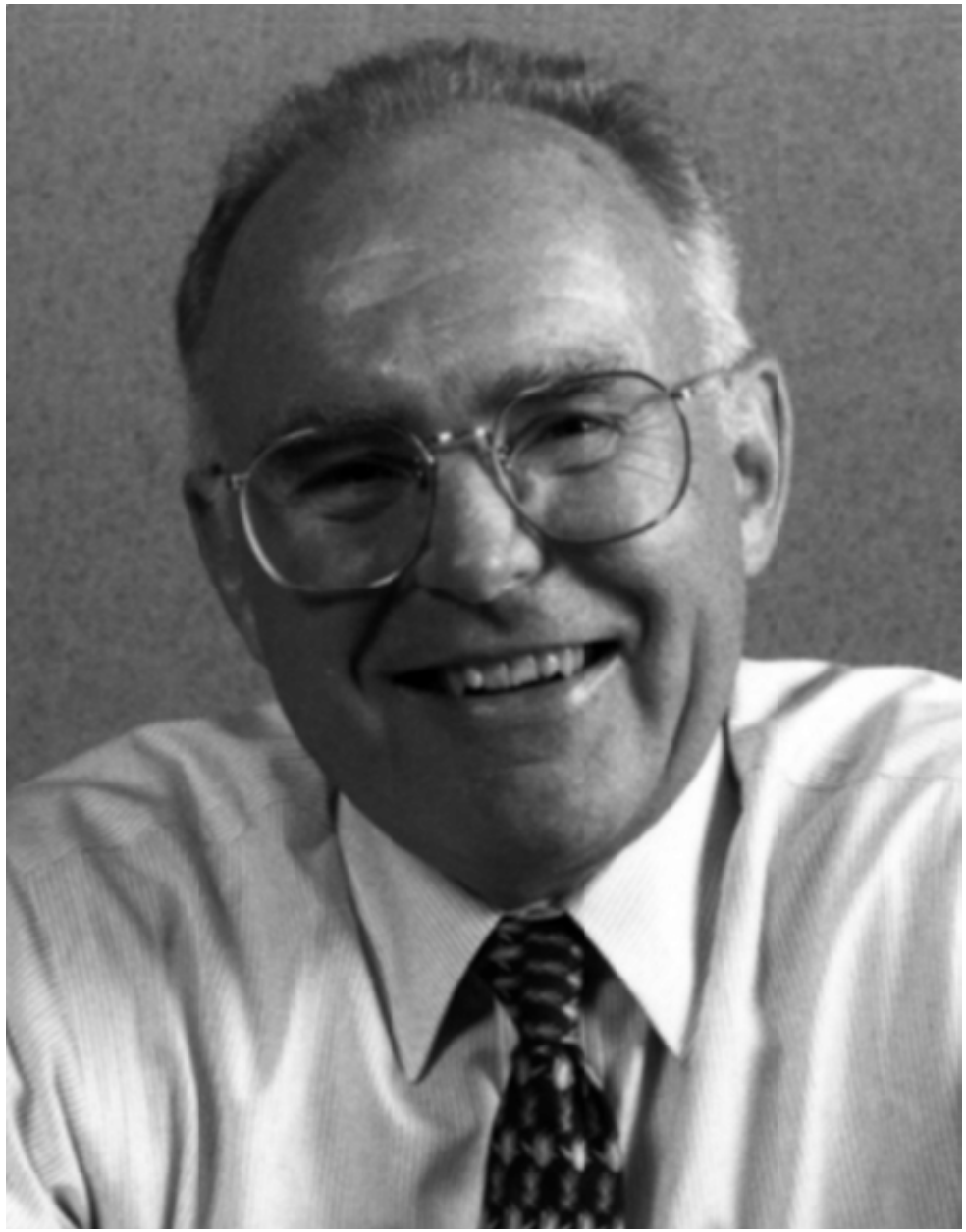
Pervasiveness of Microelectronics Revolution

- Learning curve (Haggerty)
  - Market elasticity (1960's …)
- Moore & device scaling (Dennard –1968 -1T/1C DRAM cell)
  - Moore's Law
    - Number of transistors per chip doubles every year (1965)
      - Technology: Feature reduction
      - Design: Reduction in number of transistors per memory cell from 6 (SRAM) to 1.5 (DRAM)
    - Number of transistors per chip doubles every two years (1975)
      - Technology: Feature reduction
      - Design: No more reduction in transistors per memory cell possible. Benefits derived only from improvements in layout
- Industrial concern in mid '90s as regards fab economic constraints might reduce return on capital investment
- Int'l Technology Roadmap for Semiconductors (ITRS)
  - Focus to ensure Moore's law by realizing the roadmap
  - Expansion of economy (GWP) - market elasticity (2000's) - accommodates IC CAGR

Pat Haggerty (left)

Courtesy of Fred Seitz

Gordon Moore



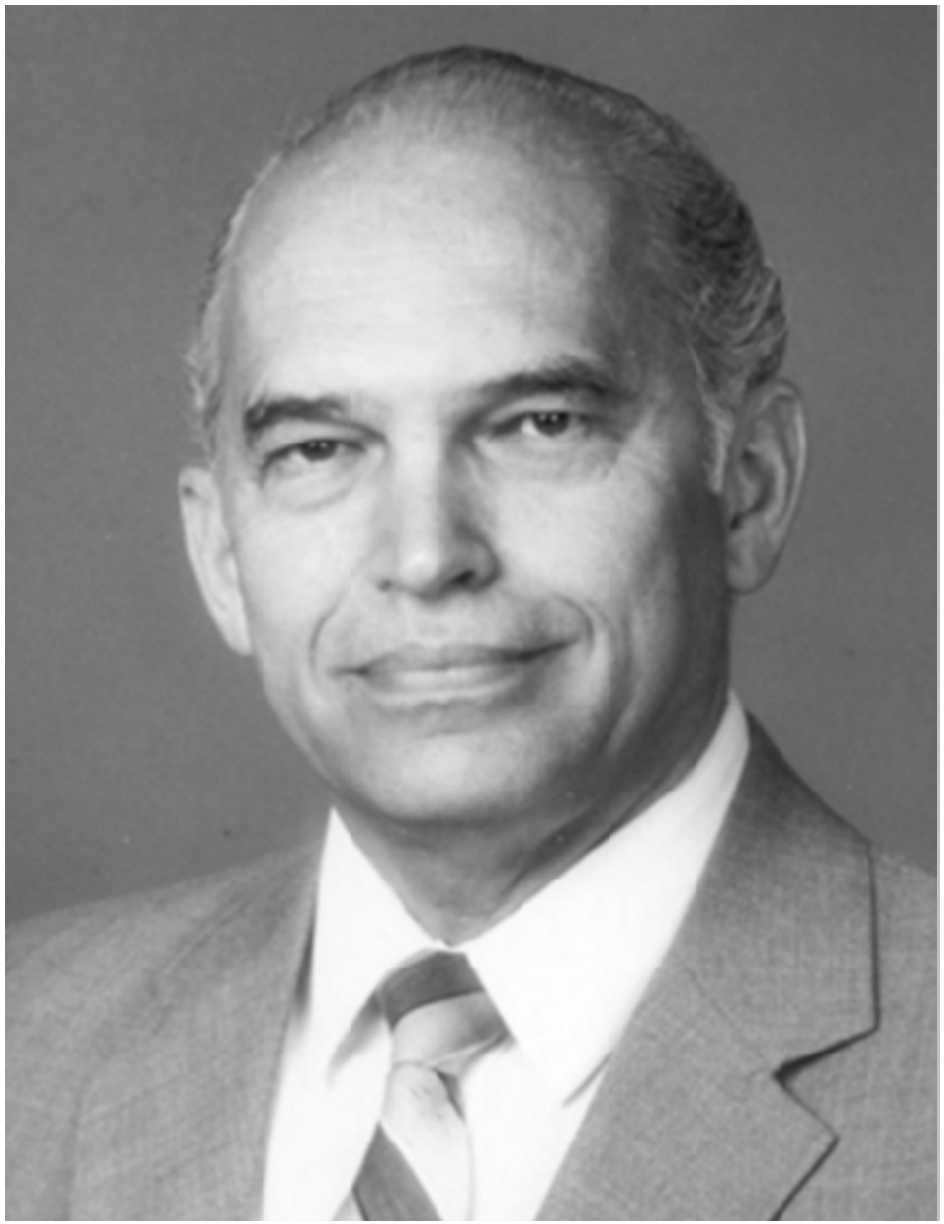
Agenda

- Introduction
- Threshold events
- Transistor Fabrication
  - Point-contact
  - Grown-junction
  - Alloy formation
  - Diffusion
- Mesa and planar advances
- Integrated circuit beginnings
- Bipolar and DRAM IC Issues
  - (1960-1980's)
- Prognosis
- Acknowledgements

Partial List Bipolar and DRAM IC Issues (1960-1980's)

- **Deal and Grove – oxidation kinetics**
  - **Hess, Irene, Massoud, Raider, Williams, Revesz, Schnable**
- **Snow, Grove, Deal and Sah – device reliability and Na contamination in SiO_2**
- **Balk – surface state passivation**
- **Dalton and Dorbek – Si_3N_4 overlayer seal against Na**
- **Kerr and Young – utilization of PSG deposited on top of SiO_2 to getter Na and K and stabilize SiO_2**
- **Snow, Deal, Balk and Eldridge – threshold voltage shifts induced by polarization in PSG layer could be controlled**

Bruce Deal



H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

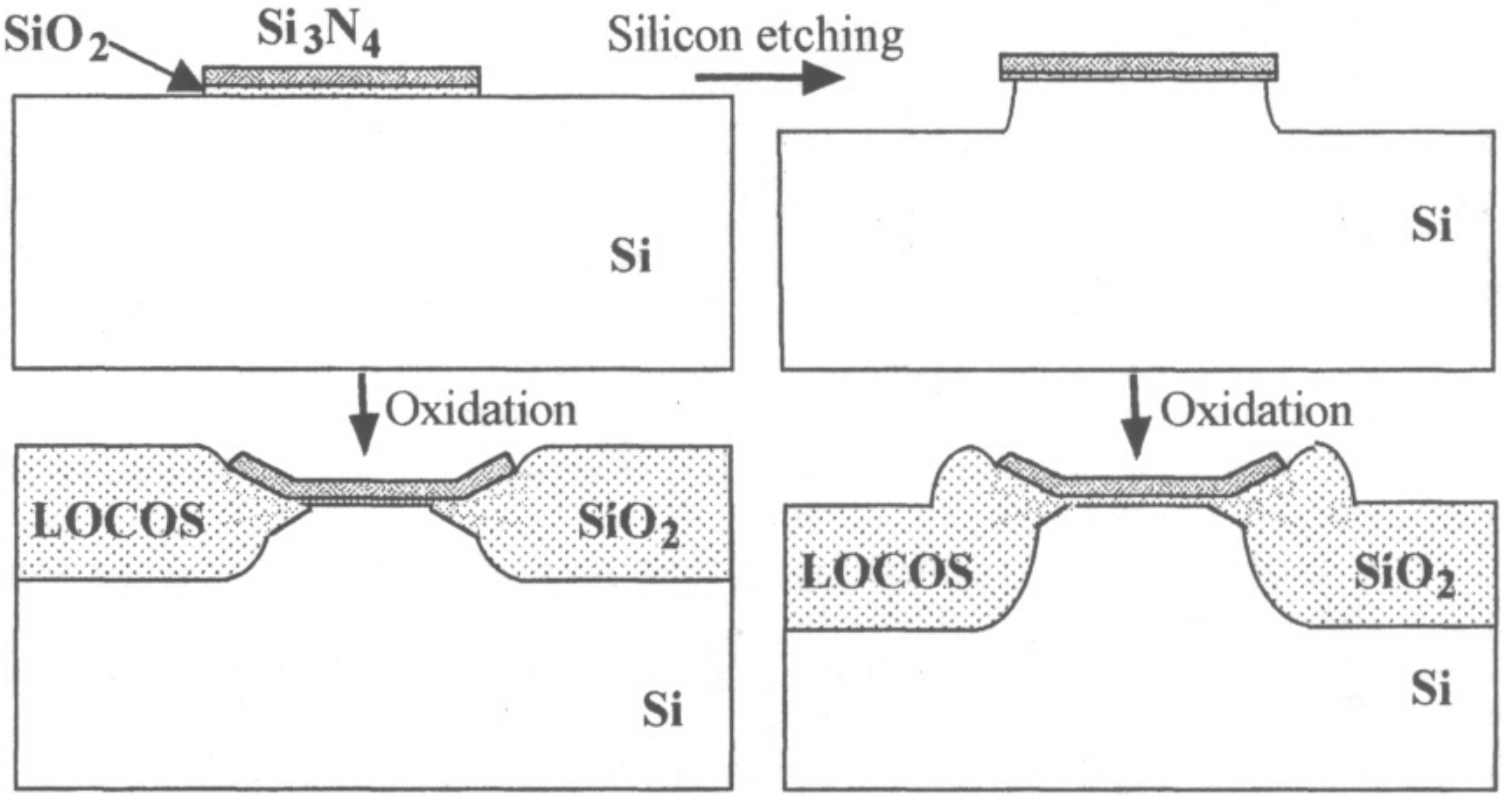
Dennis Hess

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Partial List Bipolar and DRAM IC Issues (1960-1980's) (con't)

- **Else Kooi - LOCOS**
- **Kriegler – gettering of Na by HCL in oxidation furnaces**
- **Osburn – Gate oxide integrity (GOI) and reliability via CI methodologies**
- **Reisman – VLSI laboratory proving ground**
- **Hu, Shiraki and Claeys – oxidation induced stacking fault annihilation methodologies**

Conventional LOCOS Procedures



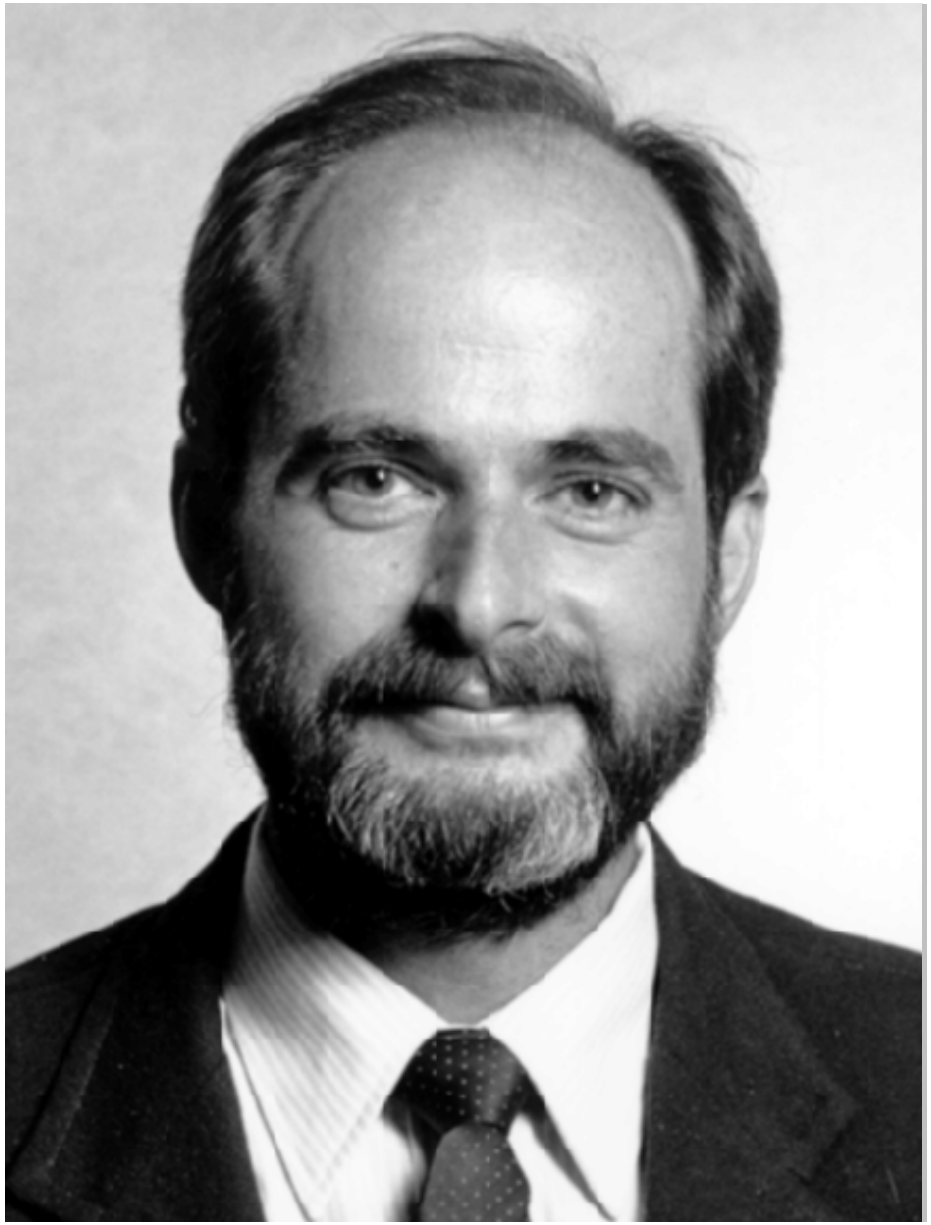
Pad oxide (SiO_2) under nitride oxidation mask relieves stress, but results in formation of "bird's beaks" at oxide edges while fully recessed oxide patterns (right) exhibit complete "bird's heads"

E. Kooi, *The History of LOCOS*, Semiconductor Silicon/1998, ECS **PV 98-1**, 200-214 (1998)
Reproduced by permission of The Electrochemical Society, Inc.

Else Kooi

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Carl Osburn

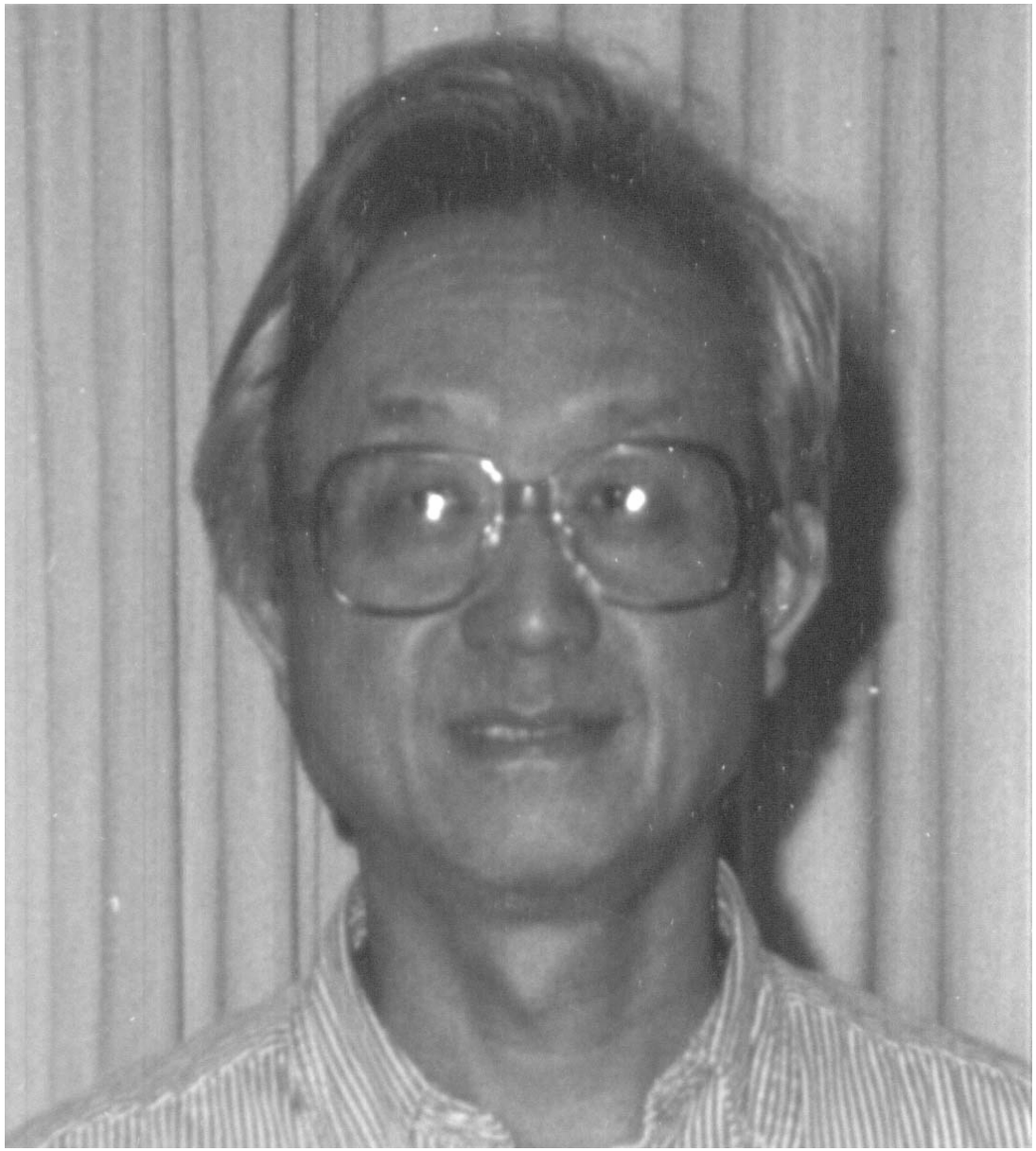


H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Arnie Reisman

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Jimmy Hu



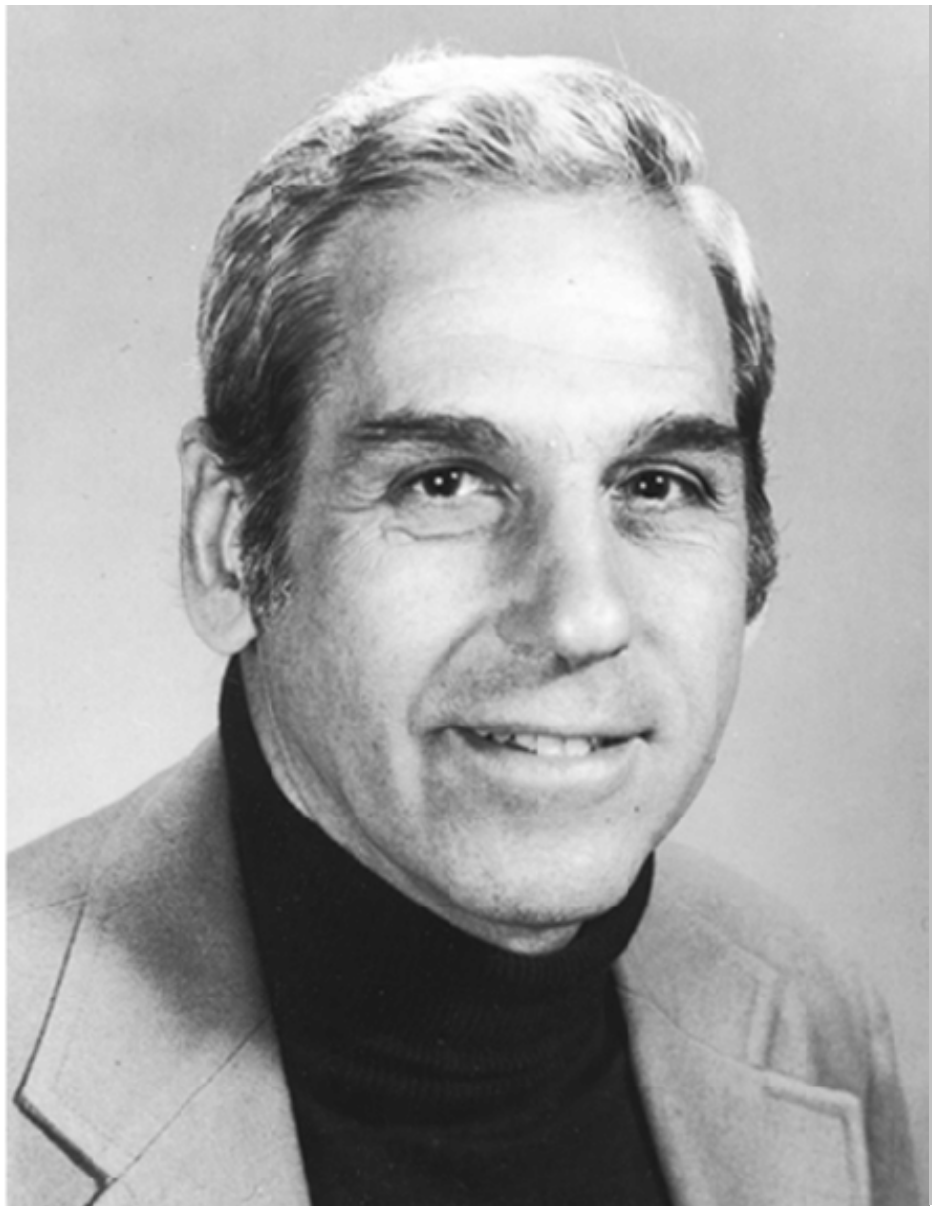
Cor Claeys

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Partial List Bipolar and DRAM IC Issues (1960-1980's) (con't)

- Moll and Termin – capacitance-voltage (C-V) analysis
- Grove, Snow, Deal and Sah – C-V analysis
- Nicollian and Goetzberger – conductance analysis
- Zaininger and Heiman – C-V for fab engineers
- Grove and Fitzgerald – p-n junction description under non-equilibrium conditions

Ed Nicollian

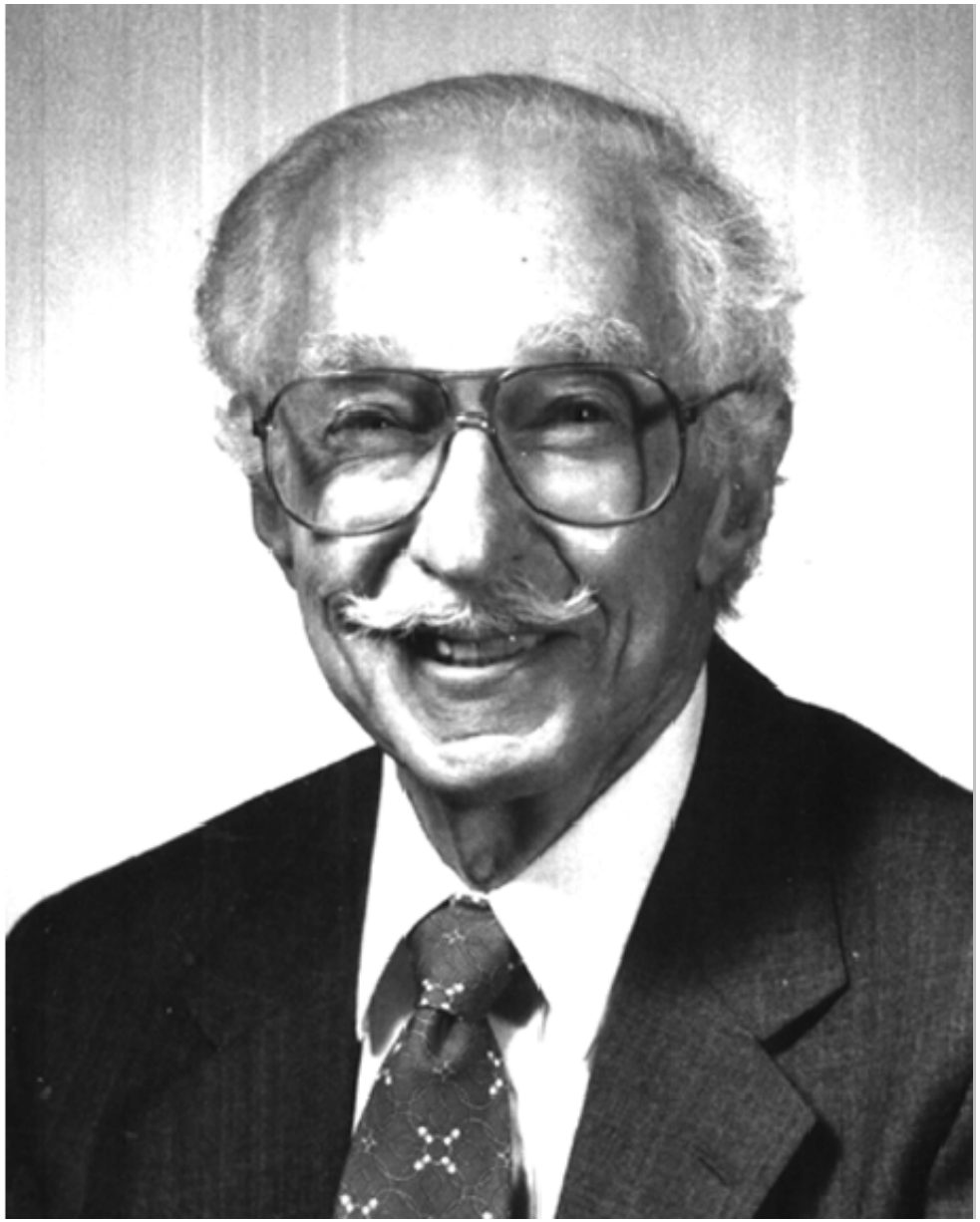


H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Partial List Bipolar and DRAM IC Issues (1960-1980's) (con't)

- **Process Issues**
  - Wafer Cleaning
  - Gold in silicon
  - Carrier lifetime
  - Plastic deformation
  - Point defects / line defects
  - Epitaxy
  - Wafer design, specifications and diameter
  - Gettering
  - GOI and related diagnostic procedures
  - Silicidation
  - Lithography, plasma etch …

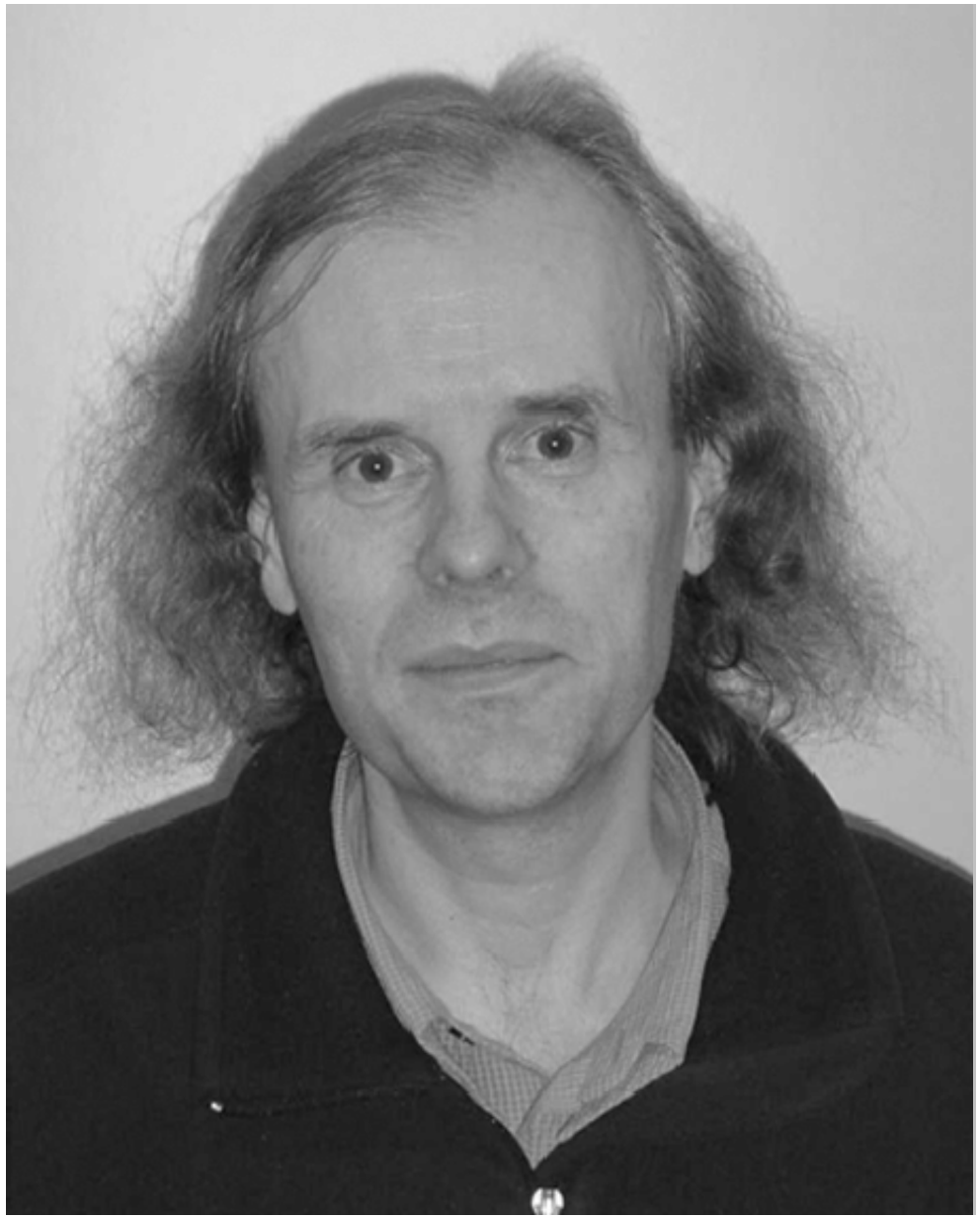
Bill Pliskin



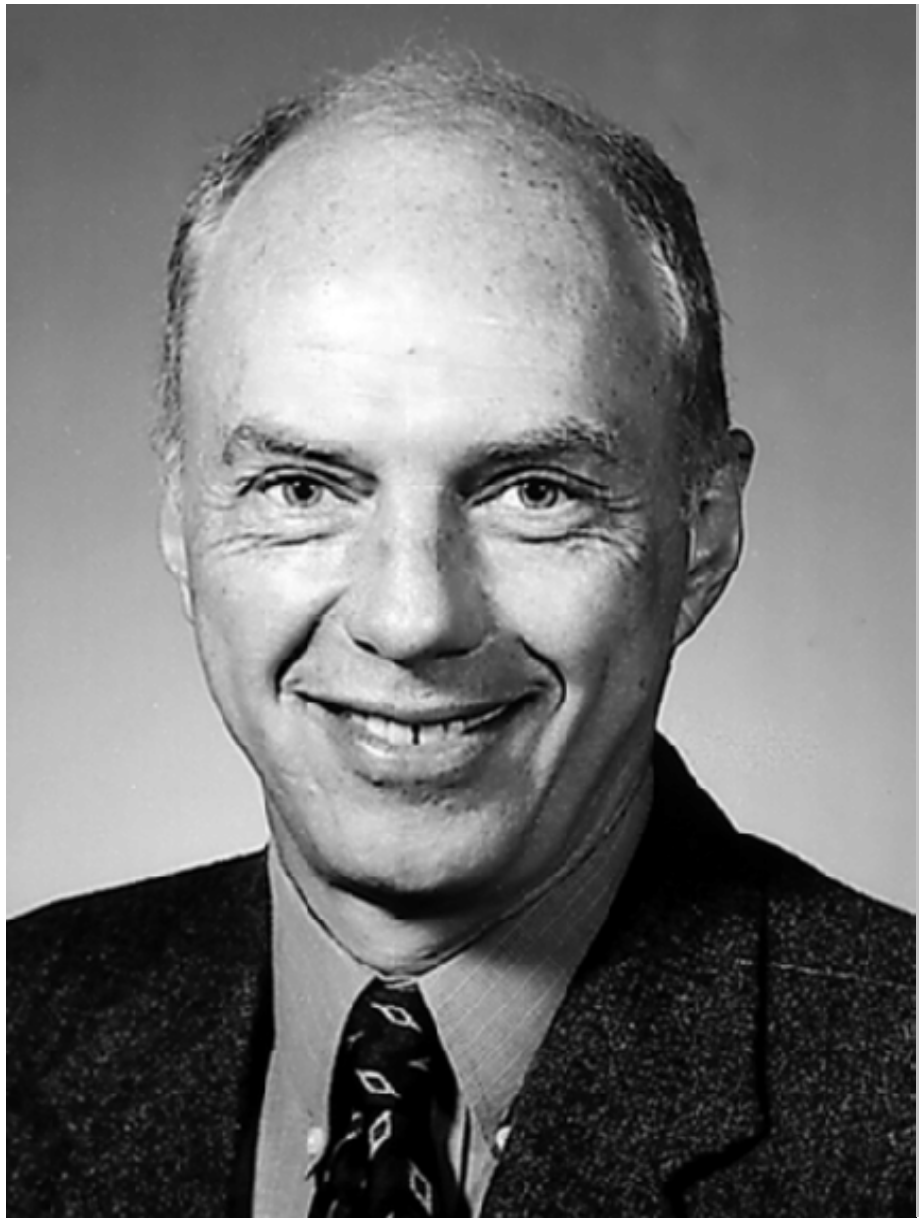
Werner Kern

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Marc Heyns



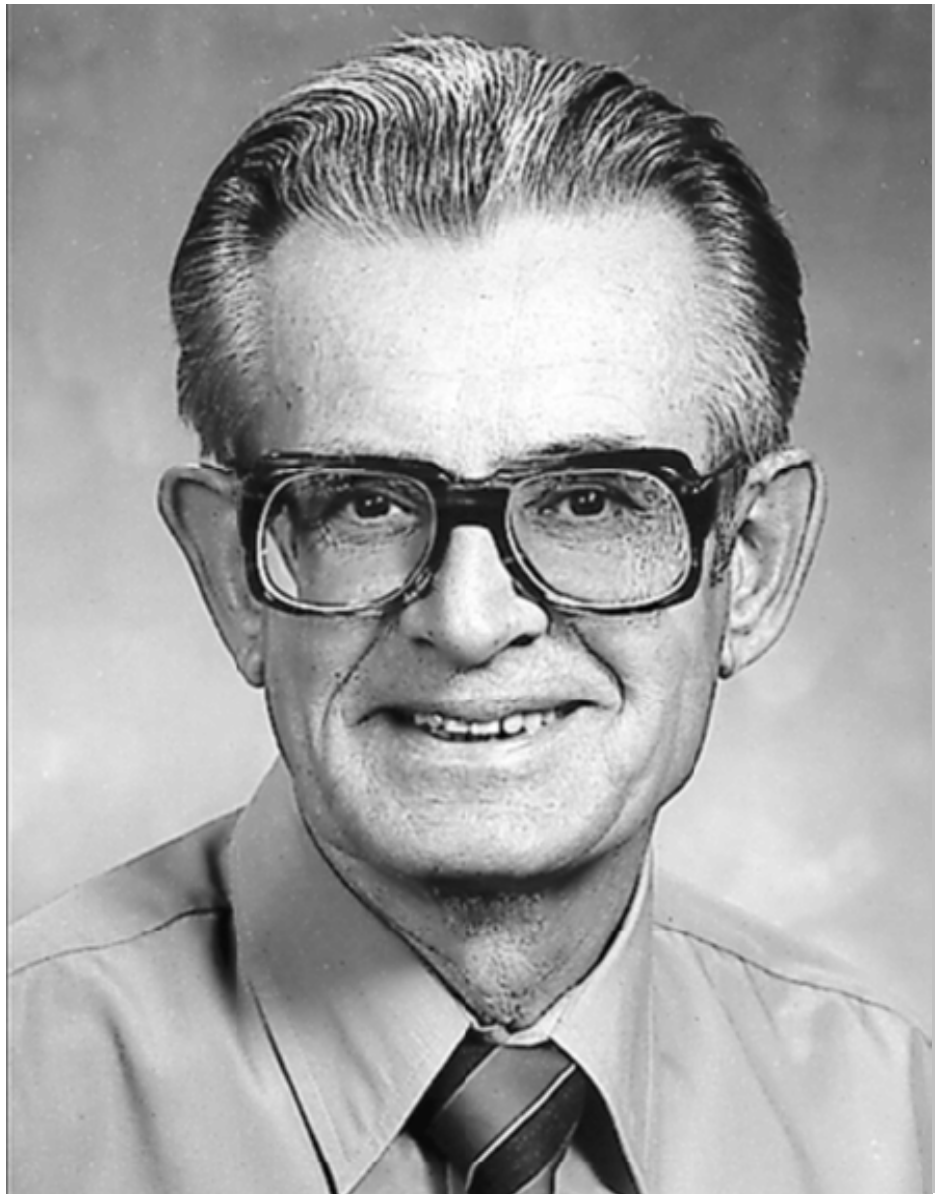
Jerry Ruzyllo



H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

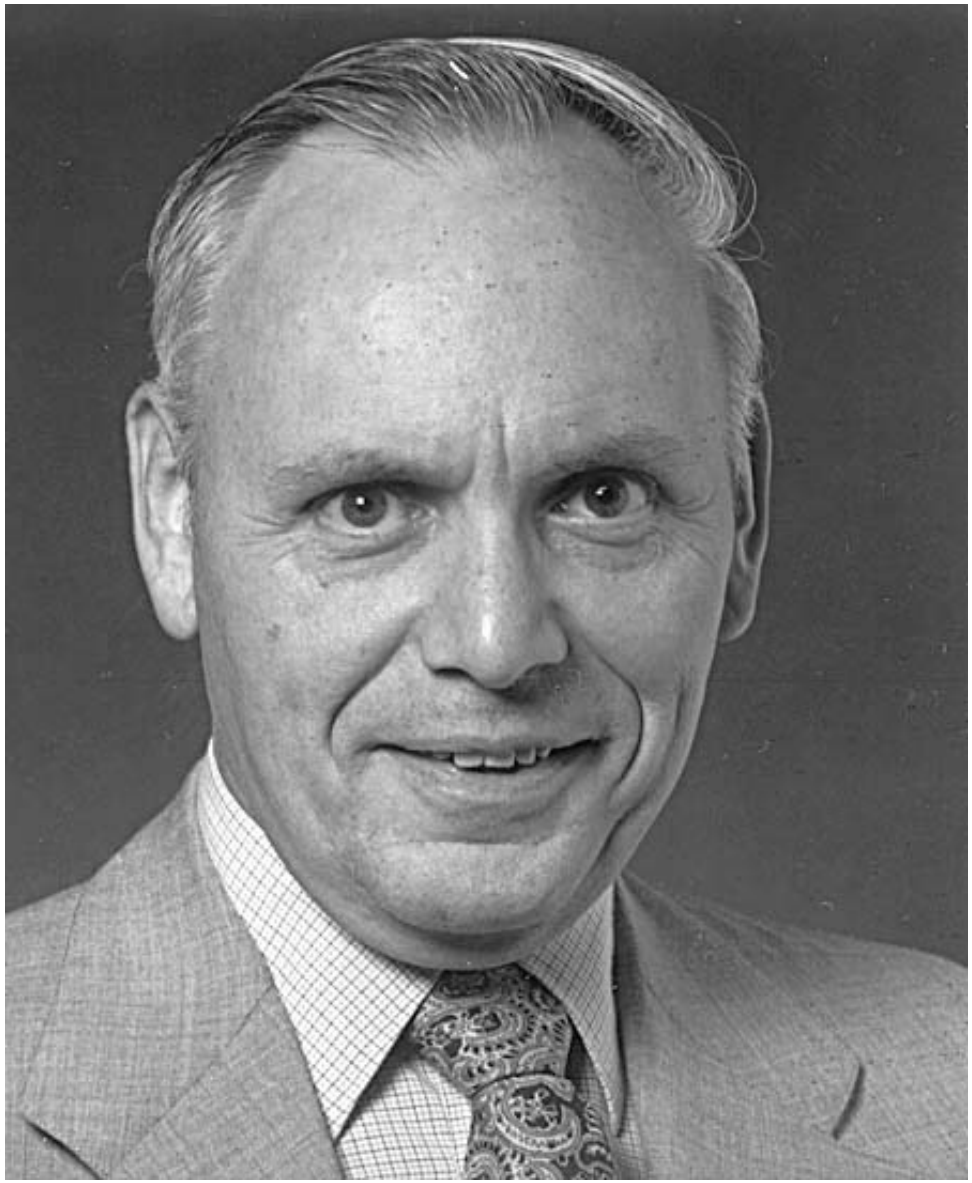
Hans Queisser

Gunther Schwuttke



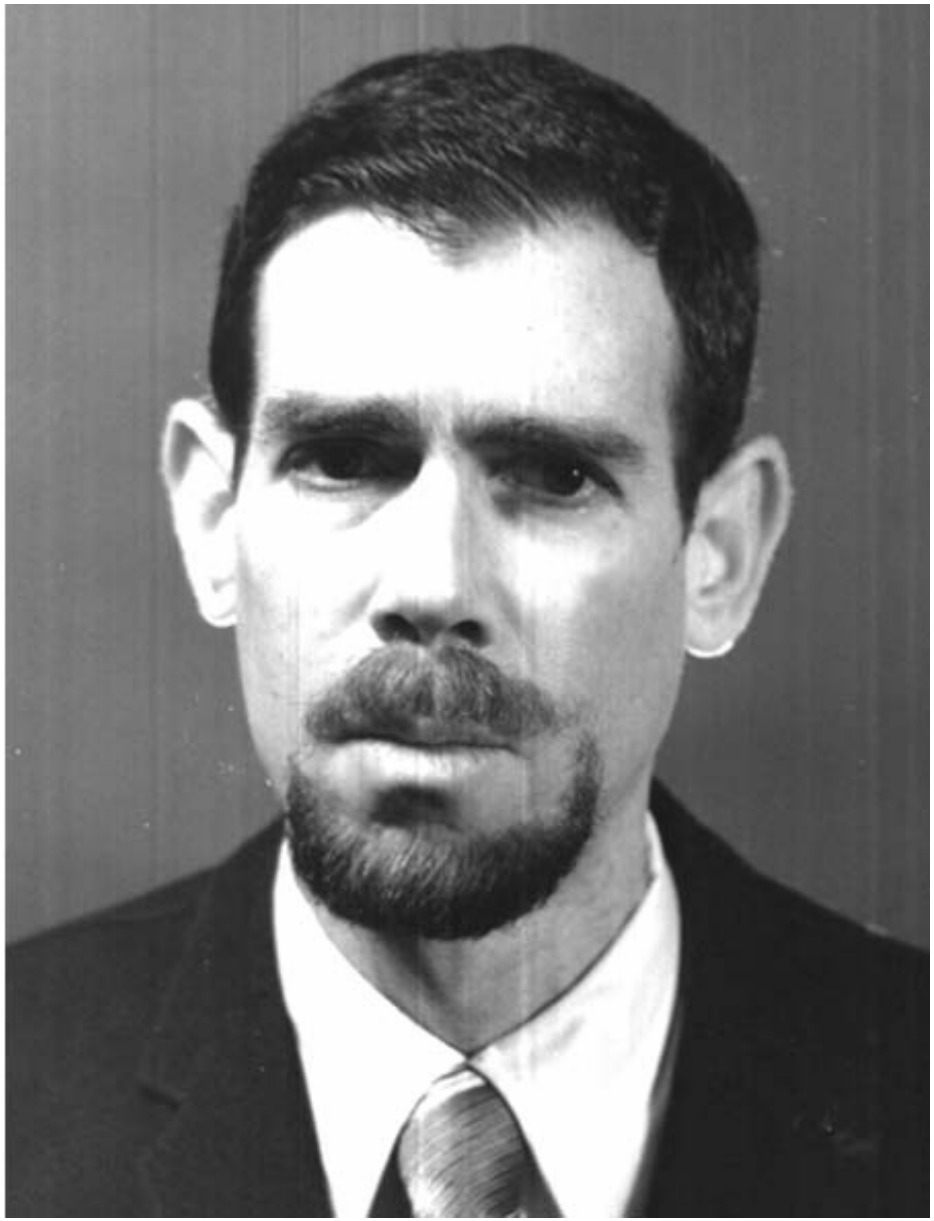
H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Jim Amick

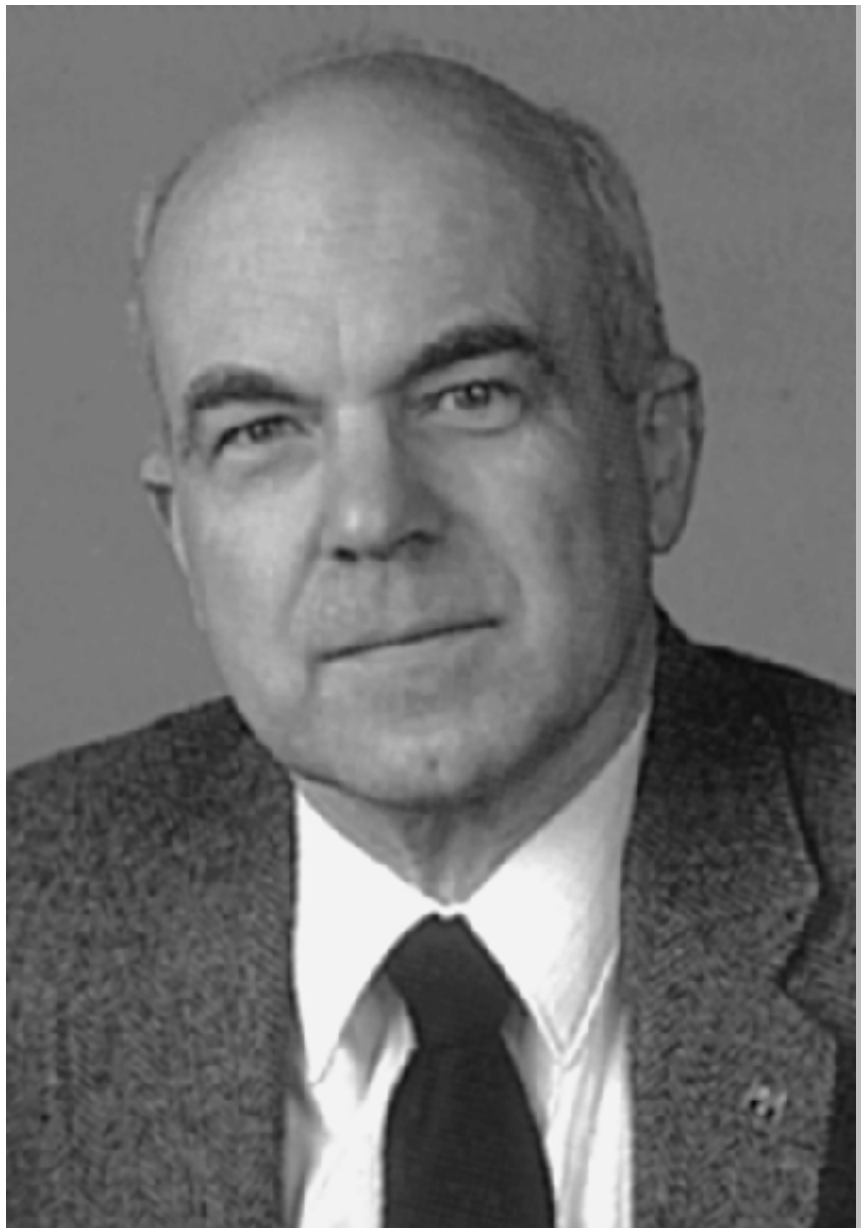


H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Ted Kamins



W. Murray Bullis



H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Eicke Weber

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Bernd Kolbesen

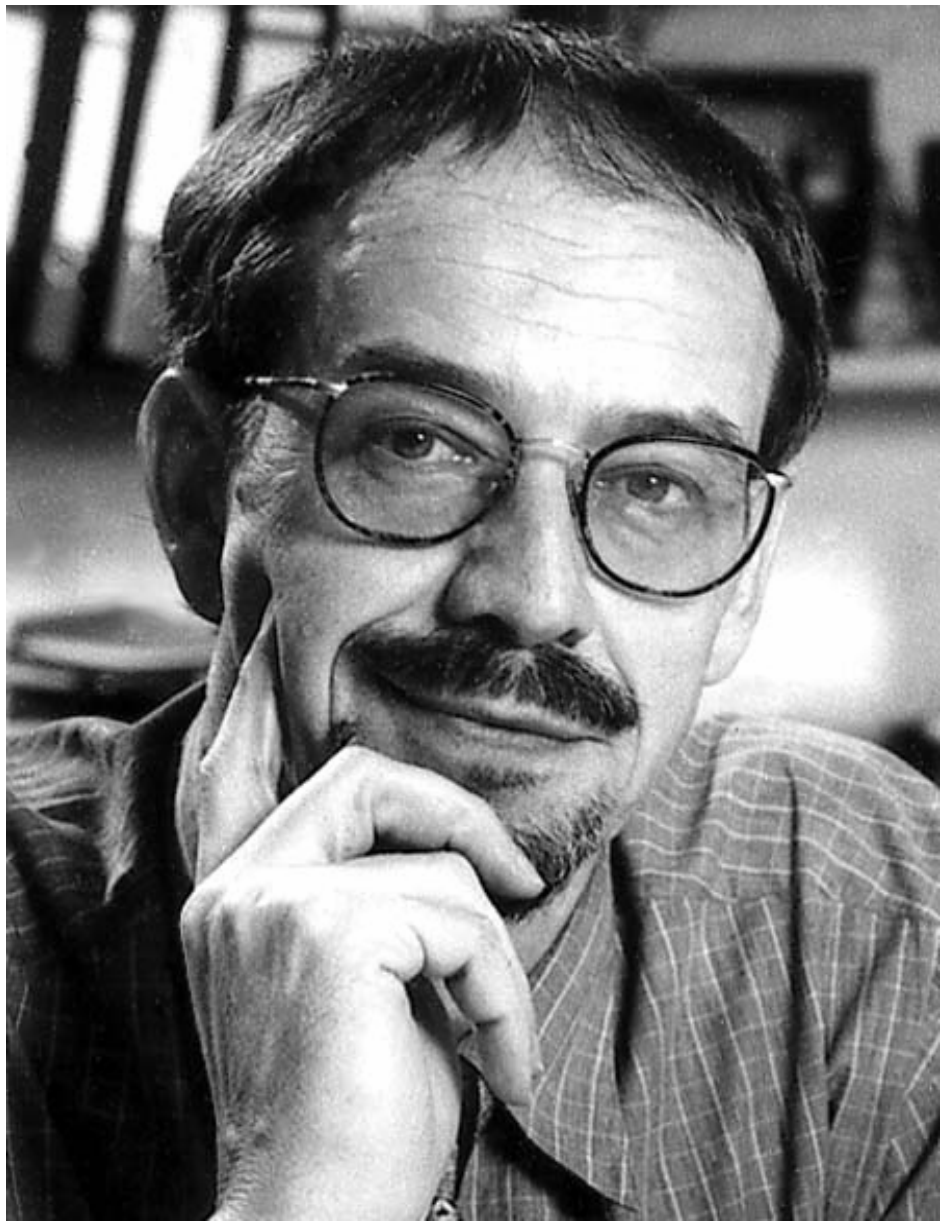
Fumio Shimura

Partial List Bipolar and DRAM IC Issues (1960-1980's) (con't)

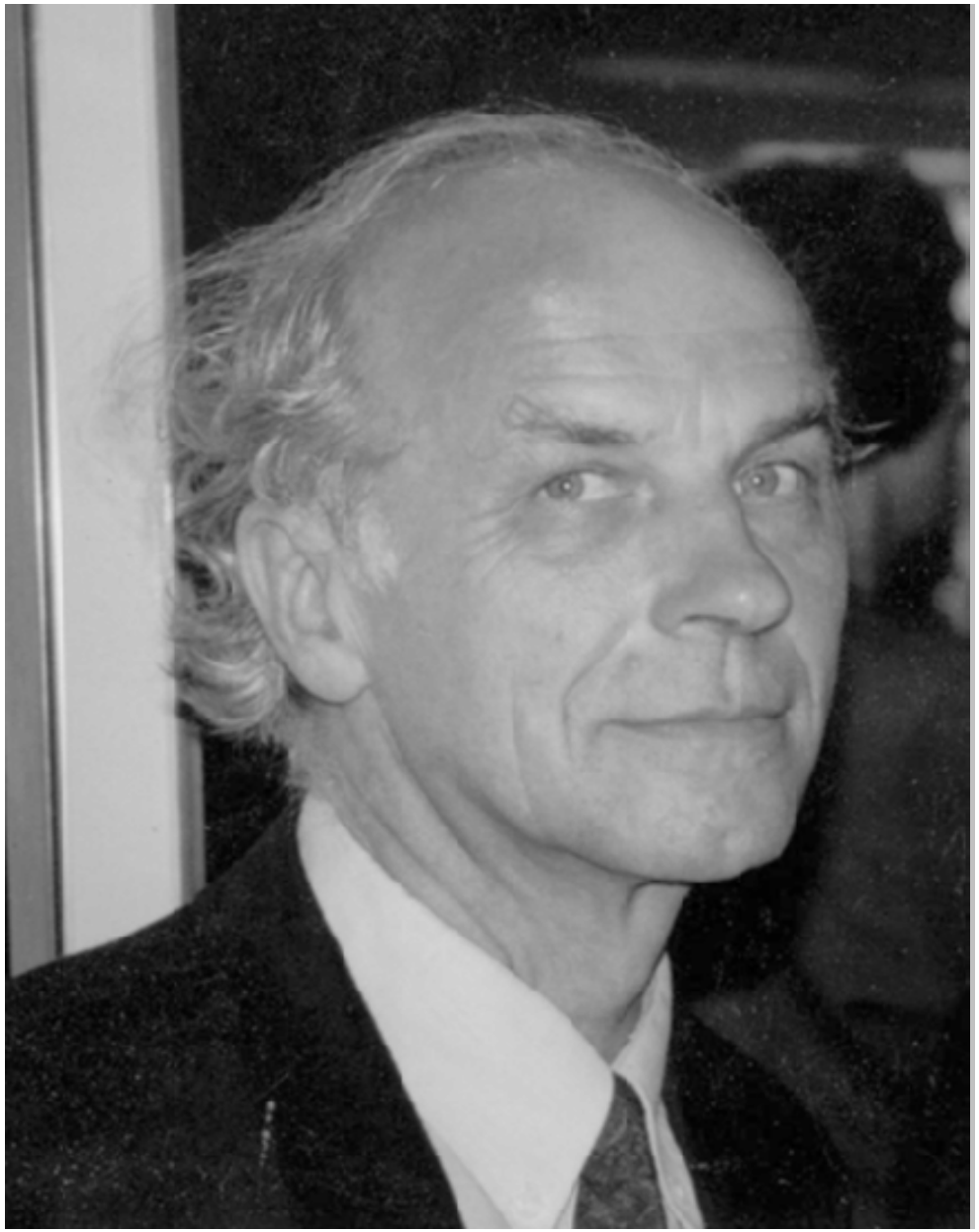
- **Tan, Gosele, Schroter, Kimerling, Plummer, Fair et al.,**
  - **Point defects**
  - **Line defects**
- **Huff / Lawrence, Takasu, Richter and colleagues**
  - **Wafer design and gettering methodologies**

Teh Tan

Ulrich Gosele



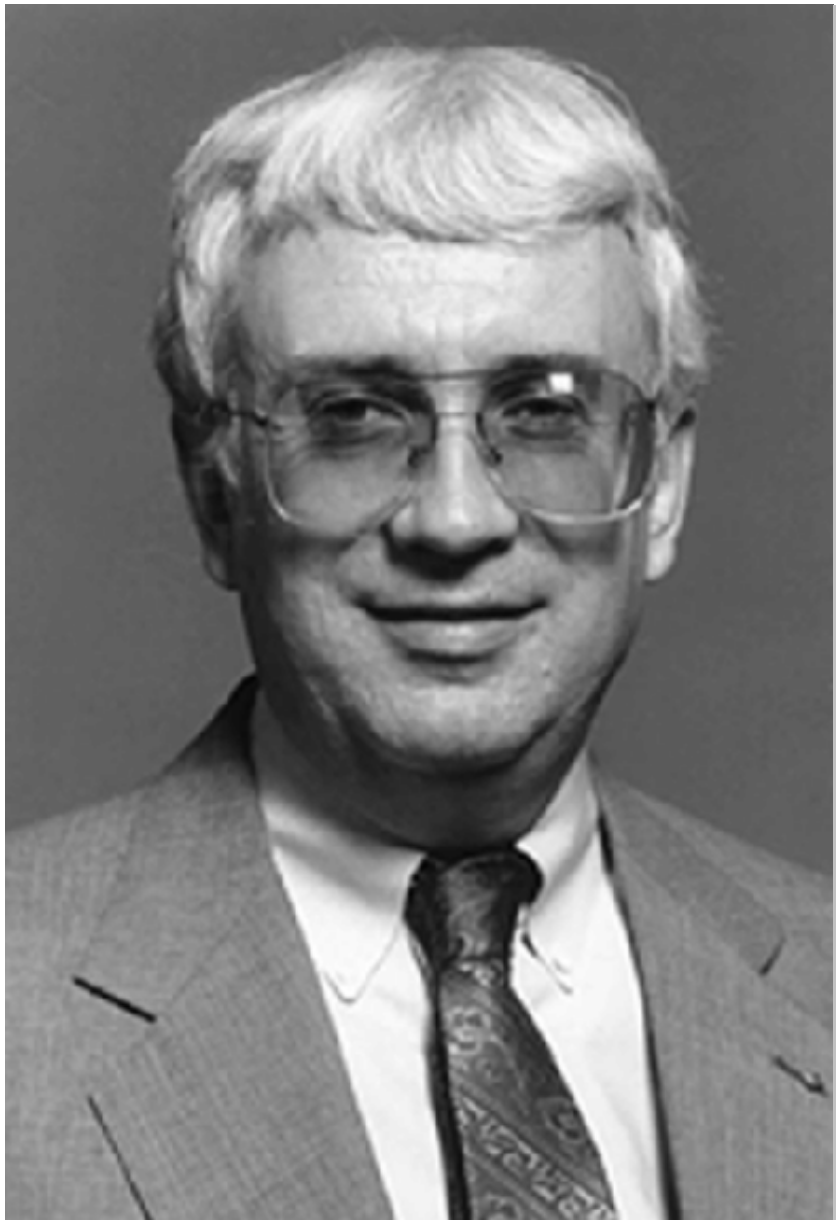
Wolfgang Schroter



Kim Kimerling

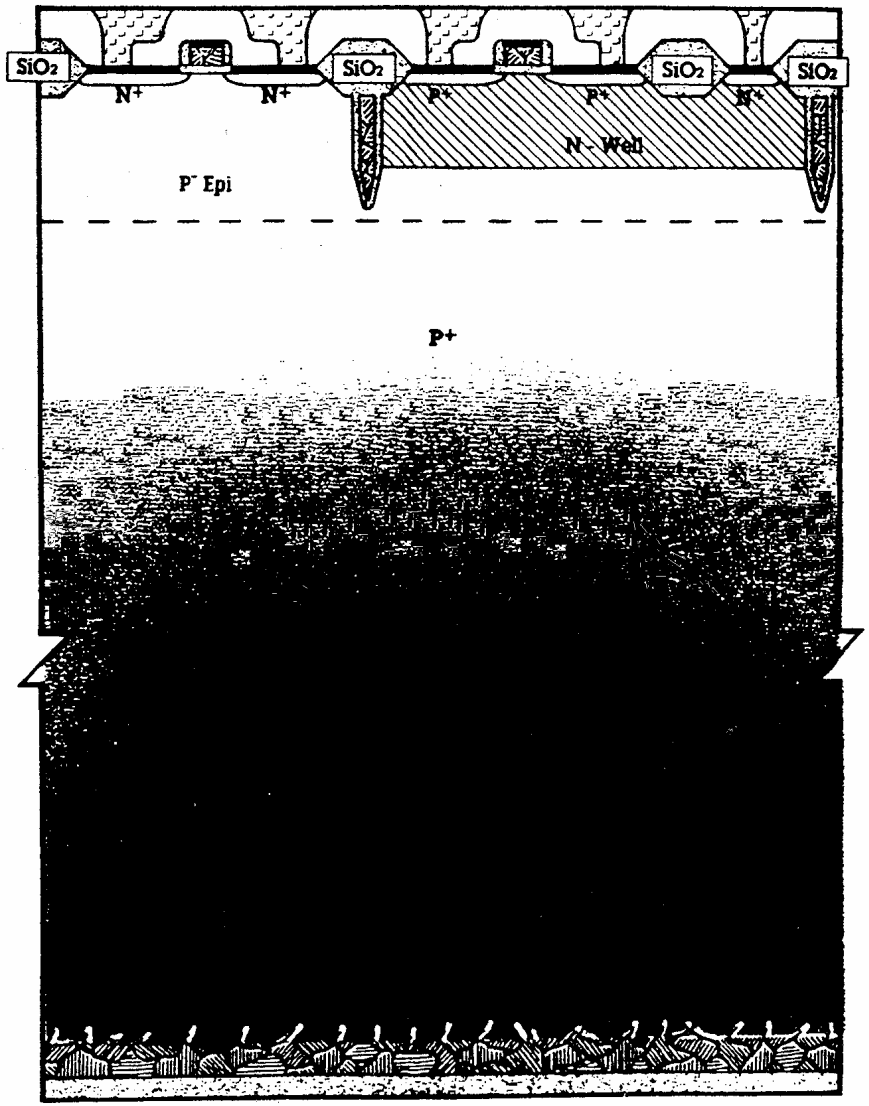
Jim Plummer

Richard Fair



H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Multi-Zone Silicon Wafer



H.R. Huff, *Silicon Wafer Product Design*,
ECS Ext. Abstracts, Abst #775,1105-1106, Fall (1987),
reprinted with permission of The Electrochemical Society, Inc.

Howard Huff

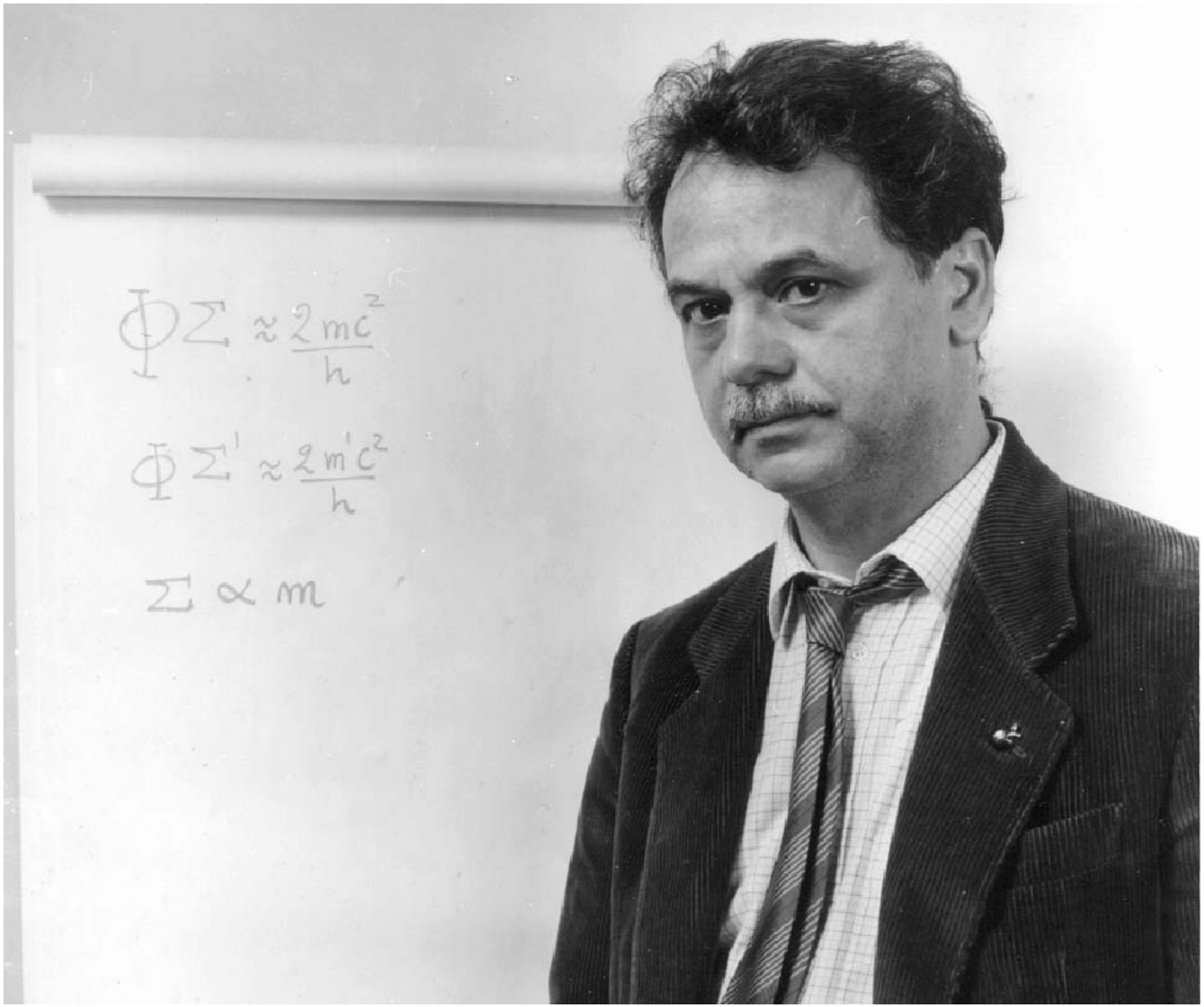
H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Shin Takasu

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Hans Richter

Geofranco Cerofolini



George Rozgonyi

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)

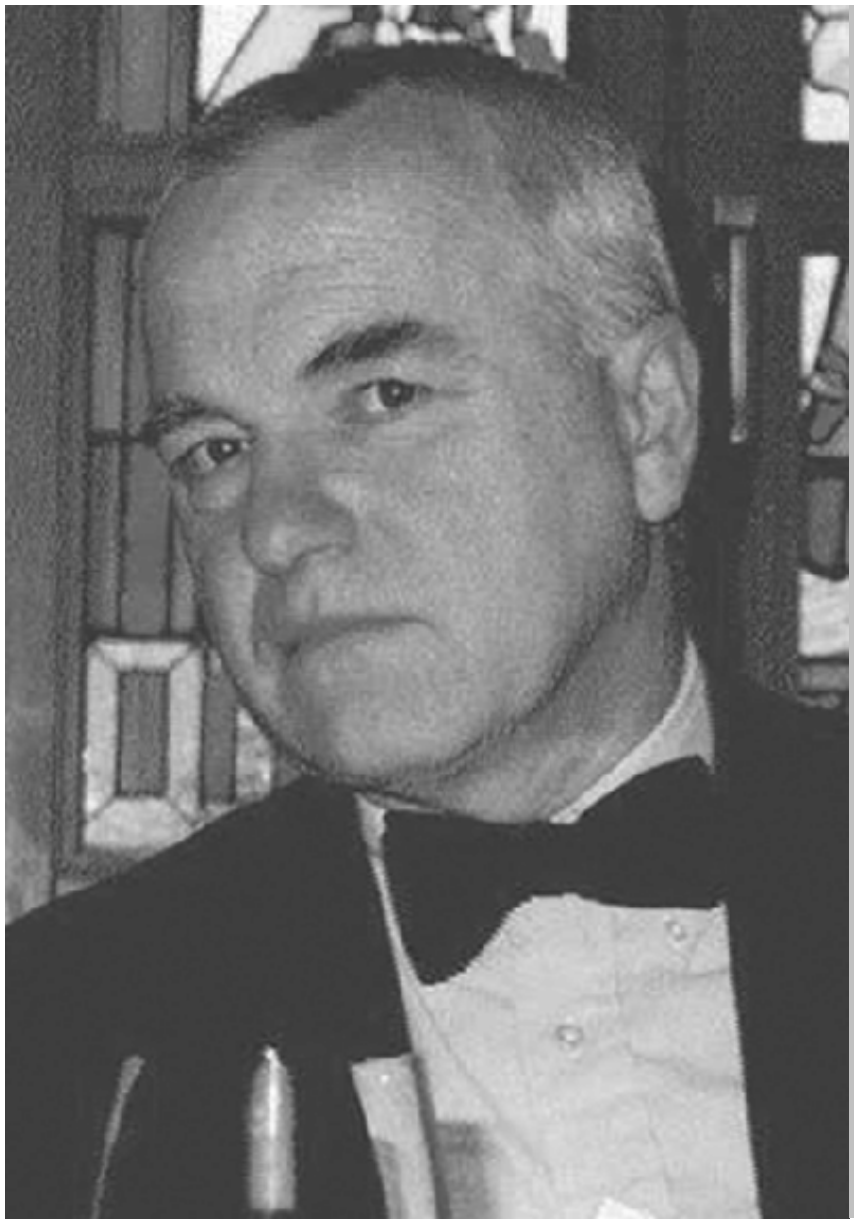
Phil Tobin

Dieter Schroder

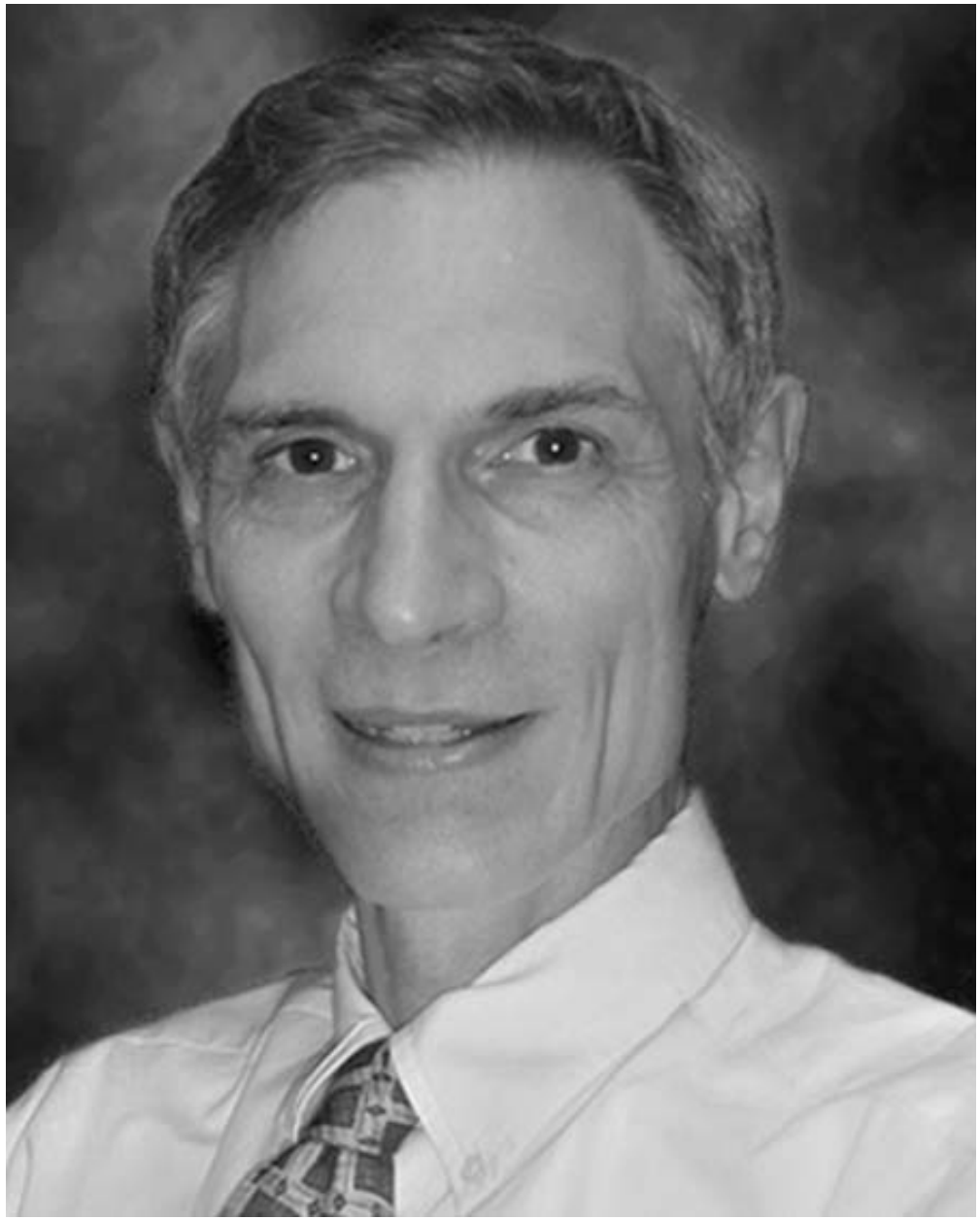
Werner Bergholz

Lubek Jastrzebski

Laszlo Fabry



Alain Diebold



Partial List Bipolar and DRAM IC Issues (1960-1980's) (con't)

- **Design Issues**
  - **Dennard - Scaling**
    - **Design rule reduction**
  - **Merged 1-T DRAM cell**
  - **Double polysilicon gate**
  - **Trench and 3D DRAM storage cell configurations**
- **Process / design optimization**

Bob Dennard

Dennard's Generalized Scaling Approach

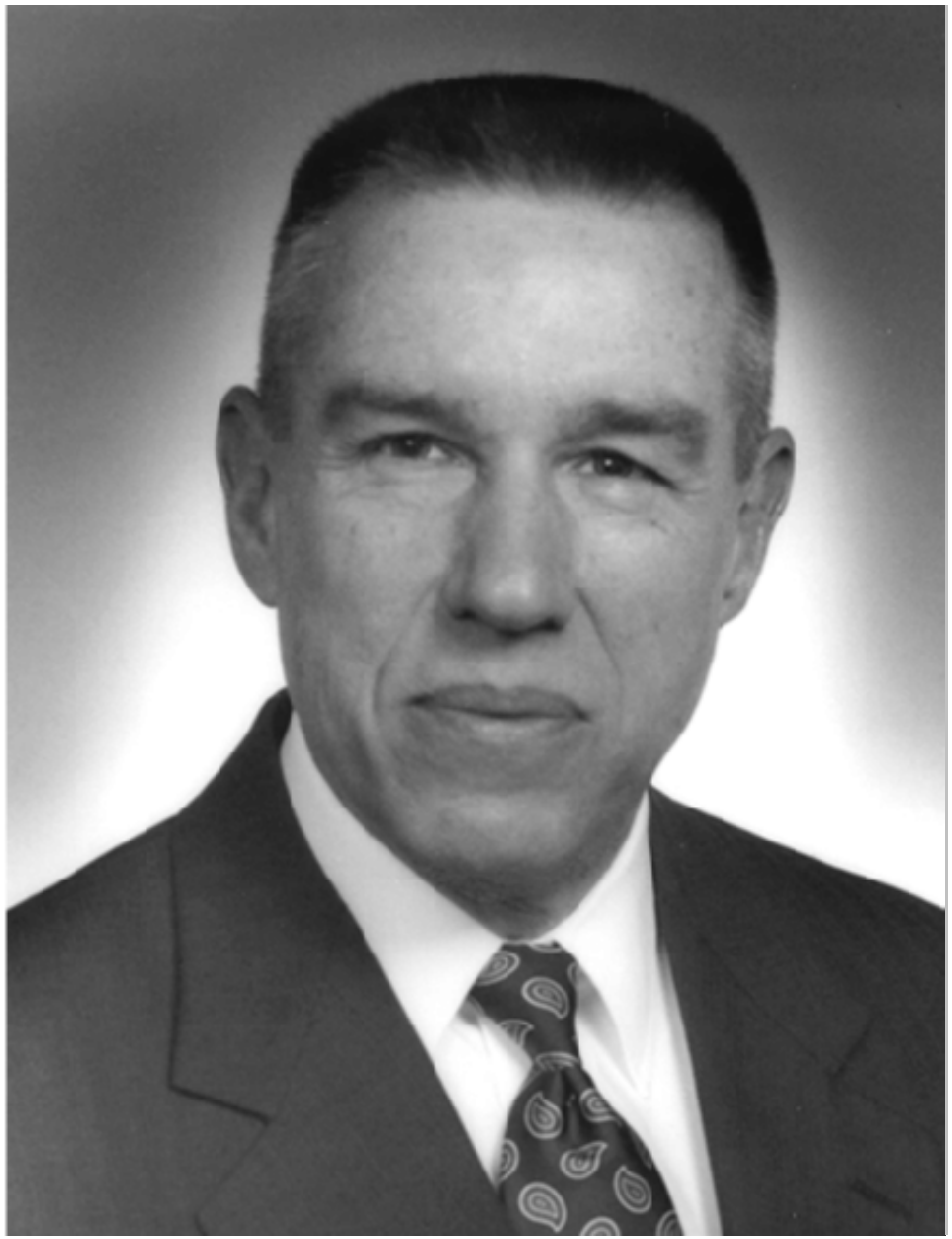
Physical Parameter	Generalized Scaling Factor
Channel length, L_g	**$1/\alpha_d$**
Gate insulator, T_{OX}	**$1/\alpha_d$**
Voltage, V	ε / α_d
Wiring Width	**$1/\alpha_w$**
Channel Width, W	**$1/\alpha_w$**
Circuit Speed (goal)	α_d
Circuit Power	$\varepsilon^2 / \alpha_d \alpha_w$

Following R.H. Dennard in *ULSI Science and Technology*, ECS **PV 97-3**, 519-532 (1997)

Al Tasch

H.R.Huff,J. Electrochem. Soc., **149**, S35-S58 (2002)
(© The Electrochemical Society, Inc., reproduced with permission)

Jim Meindl

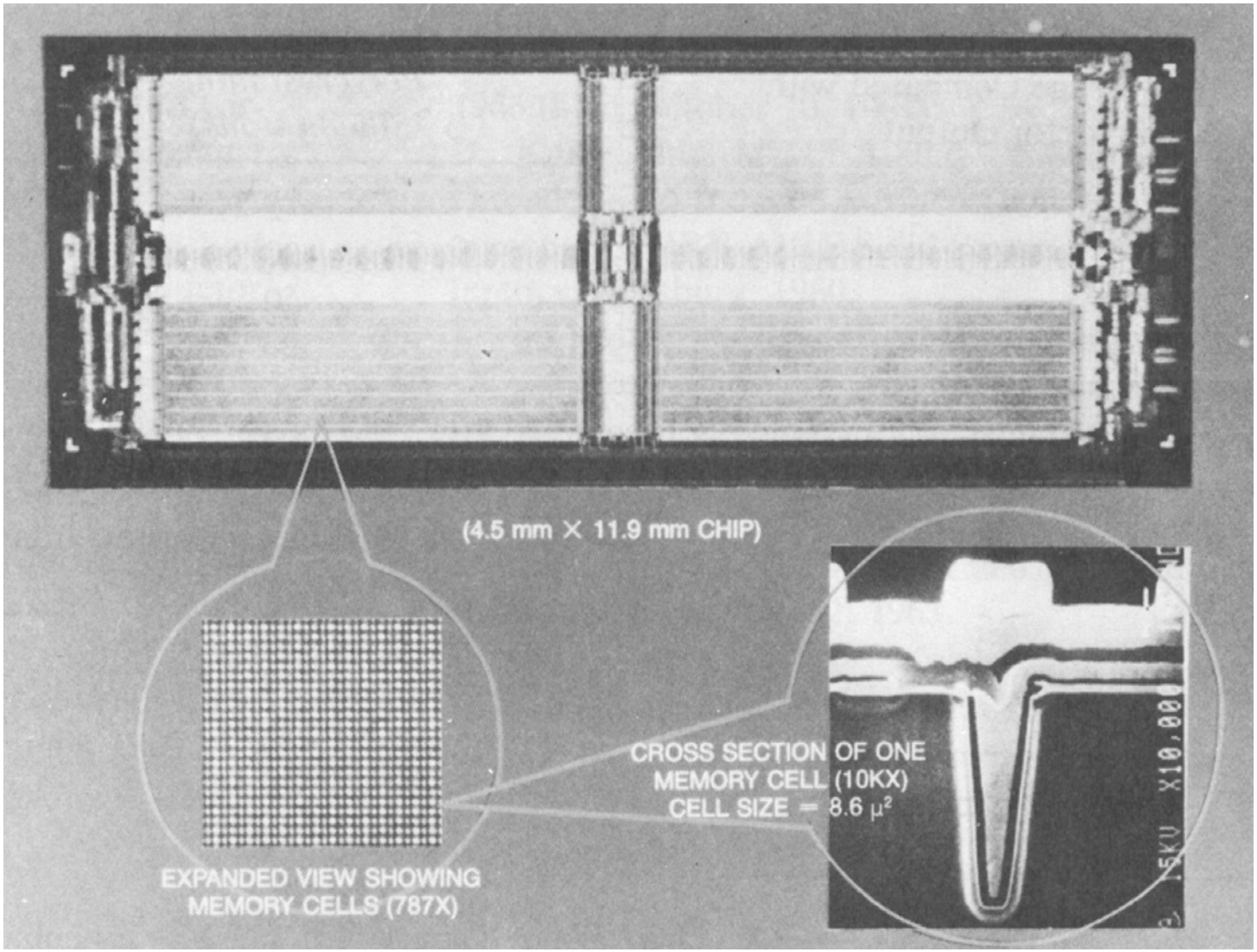


DRAM Process and IC Evolution (circa 1992)

Parameter	Units	ULSI	VLSI	LSI	MSI
Bits/chip	Number	10^7 - 10^9	10^5 - 10^7	10^3 - 10^5	10^2 - 10^3
Design Rule	μm	< 1	1 - 3	3 - 5	5 - 10
Power-delay product	PJ	< 10^{-2}	10^{-2} - 1	1 - 10	10 - 10^2
Mask levels	Number	15 – 20	8 – 15	6 –10	5 – 6
Chip area	mm^2	50 – 280	25 – 50	10 – 25	10
Storage cell (equivalent oxide thickness)	(nm)	3.5 - 12.5	12.5 - 40	40 - 90	90 - 120
Junction depth	μm	0.04 – 0.2	0.2 - 0.5	0.5 - 1.2	1.2 - 2

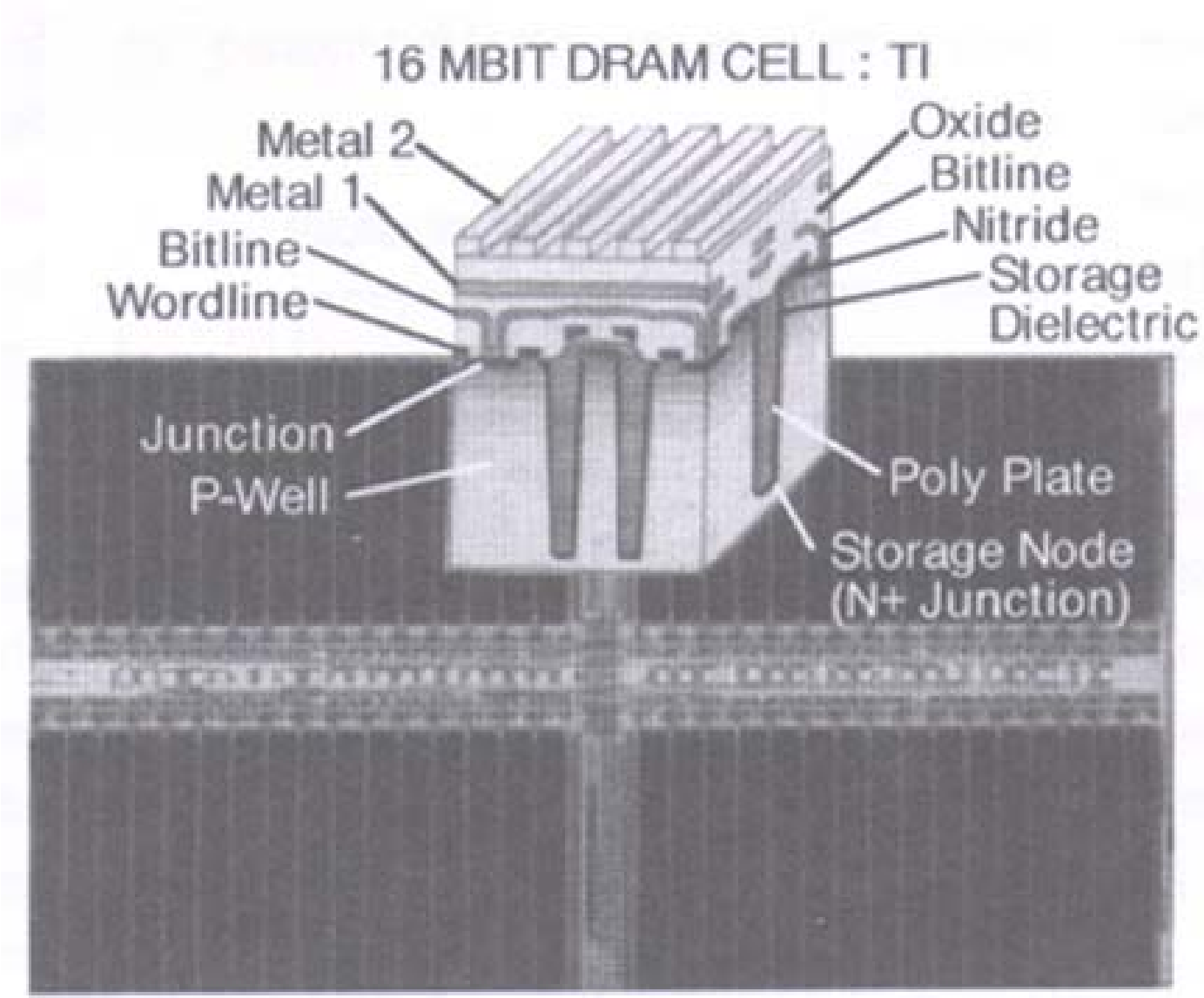
Following H.R. Huff, *Silicon: Properties and Material Specifications* in *Concise Encyclopedia of Semiconducting Materials & Related Technologies*, edited by S. Mahajan and L.C. Kimerling, Pergamon Press (1992)

One Mbit CMOS DRAM Chip



Courtesy of Texas Instruments, Inc.

16 Mbit DRAM Cell



Courtesy of Texas Instruments, Inc.

Agenda

- Introduction
- Threshold events
- Transistor Fabrication
  - Point-contact
  - Grown-junction
  - Alloy formation
  - Diffusion
- Mesa and planar advances
- Integrated circuit beginnings
- Bipolar and DRAM IC Issues
  - (1960-1980's)
- Prognosis
- Acknowledgements

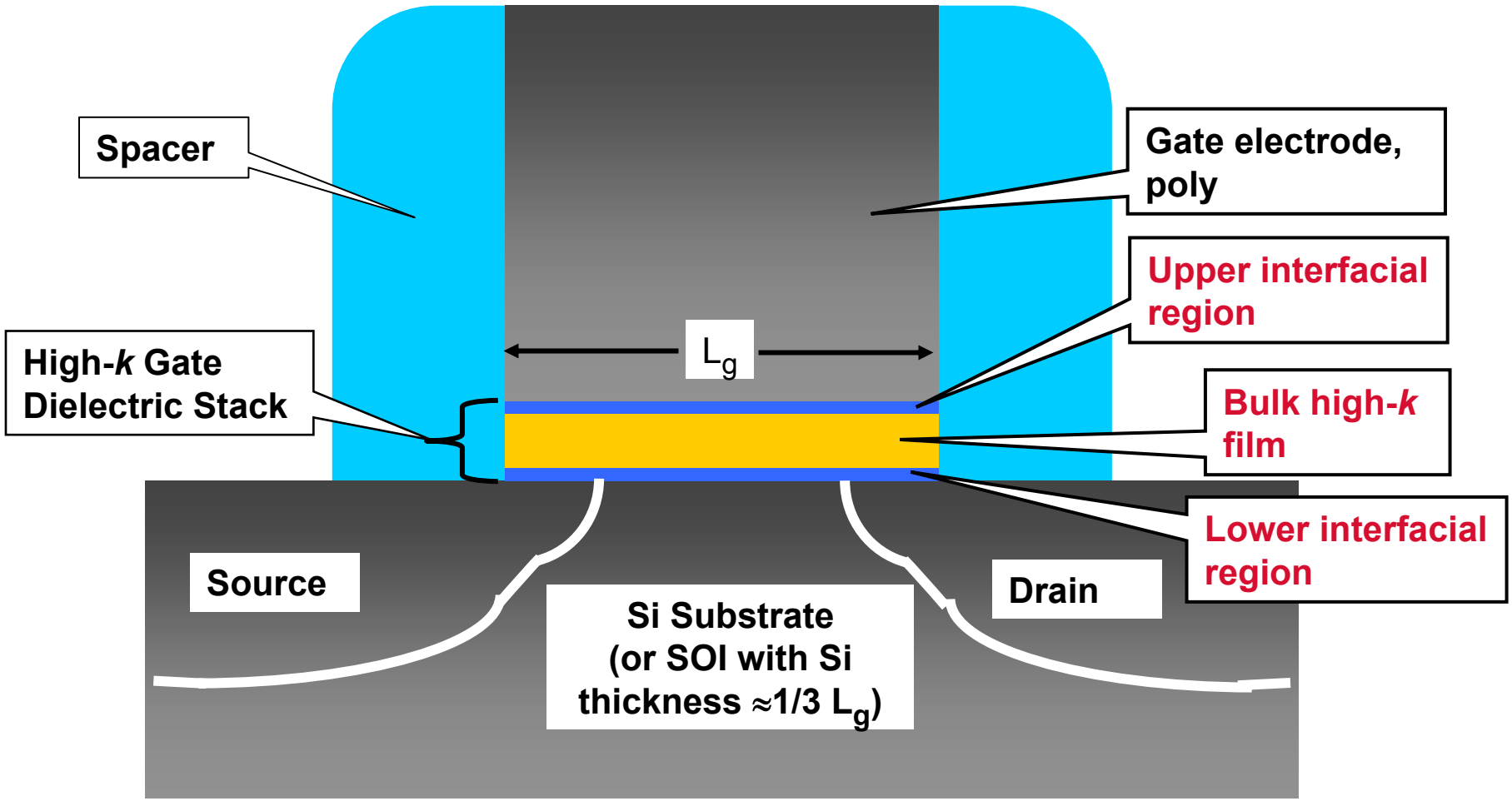
1956 Nobel Prize

Courtesy of Lillian Hoddeson

Microelectronics Revolutionaries –1998 Silicon Symposium Celebrating 50th Anniversary of Commercialization of Point-Contact Transistor
(Special Historical Session)

H.R. Huff, J. Electrochem. Soc., **149**, S35-S58 (2002)

Simplified Cross-Section of MOSFET Transistor Structure



Modified From P.M. Zeitzoff, R.W. Murto and H.R. Huff, *Solid State Technology*, July 2002

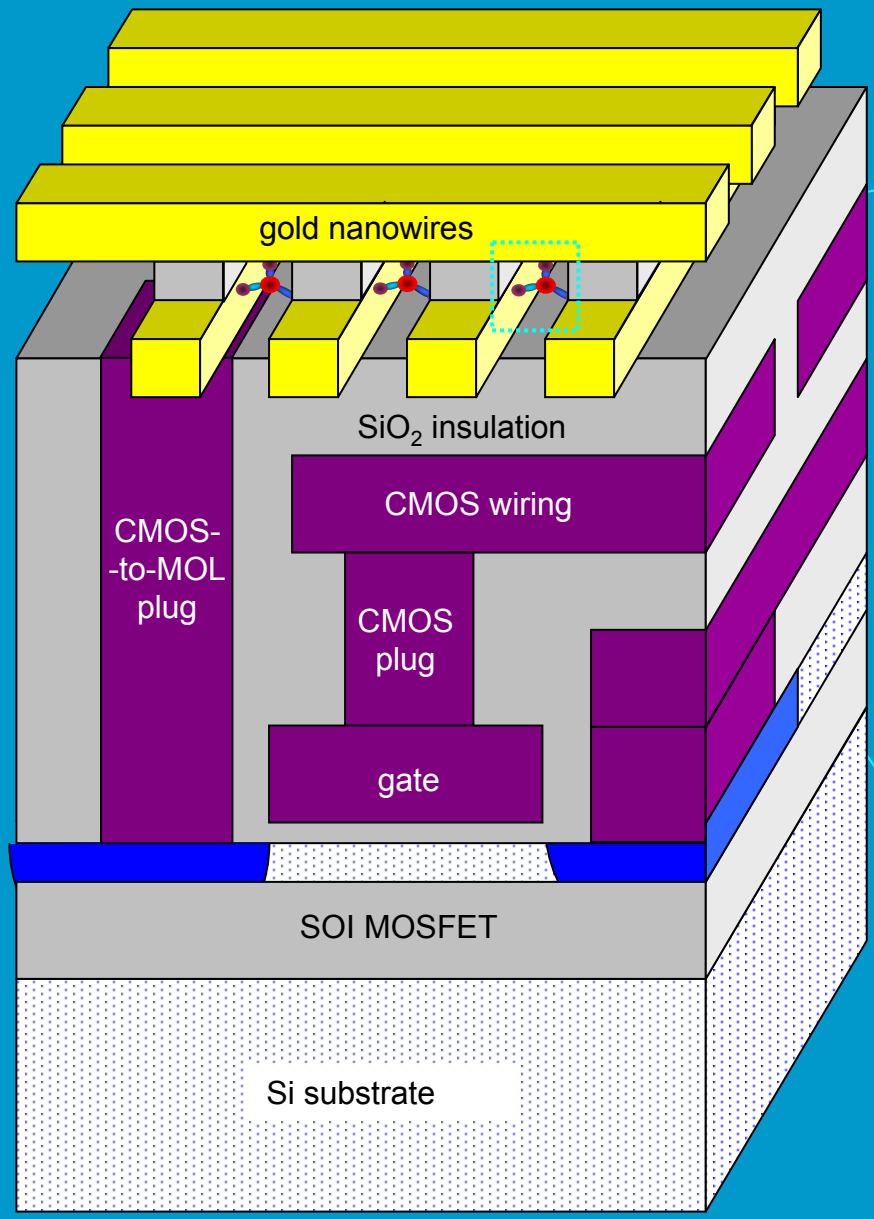
Integrated Circuit Historical Scaling Trends

- **4K DRAM (1974)**
  - SiO_2 thickness ≈ 75-100 nm
  - Channel physical length (L_g) ≈ 7500 nm
  - Junction depth ≈ several μm
    - Power supply = 5 V
- **High-performance MPU (2003) - ITRS: 100 nm technology generation**
  - SiO_2 equivalent oxide thickness (EOT) ≈ 1.1 - 1.6 nm
  - Channel physical length (L_g) ≈ 45 nm
  - Extension junction depth ≈ 25 nm
    - Power supply = 1 V

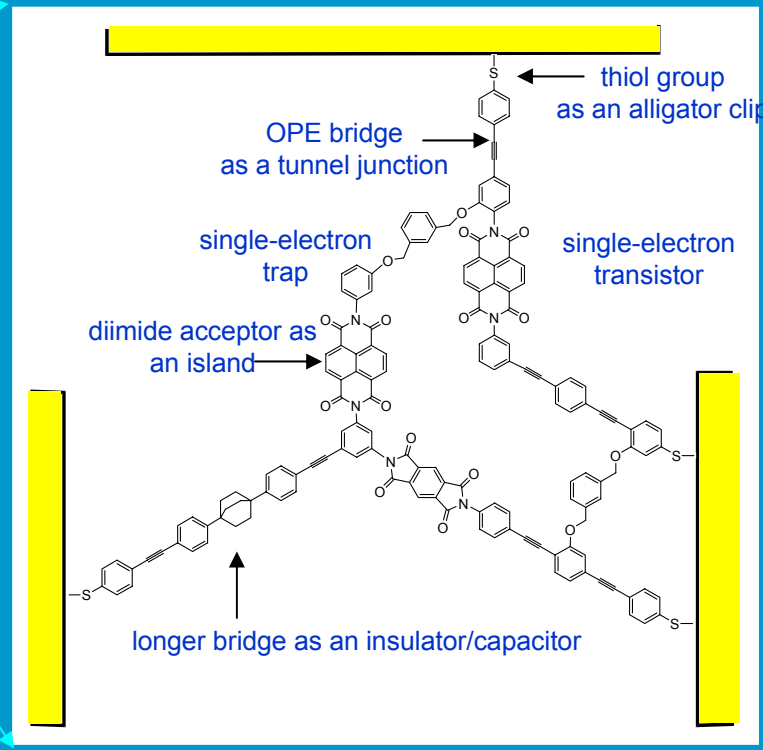
Evolving Trends of Alternative Novel Device Structures Beyond CMOS

- **Requirements**
  - Capability to be integrated with Si-CMOS
  - Room-temperature operation
  - Capability for SOC, including gigabytes of memory storage
  - Portable capability, with opportunity for large-scale market
- **Examples** (non-ranked)
  - Opto-electronic system (with multi-layered epitaxial structures)
  - Spintronics
  - Self-assembled nanostructures (including molecular structures)
  - Nanowire arrays
  - Microclusters/quantum dots in "SiO_2" (in higher-dimensional matrix)
  - Carbon nanotubes
  - Cellular automata
  - Fullerenes
  - Single-electron structures
  - Optical computers
  - DNA computers
  - Quantum computers

CMOL CONCEPT



molecular single-electron latching switch



Possible density: 3×10^{12} functions per cm^2

K. Likharev and A. Mayr, 2002

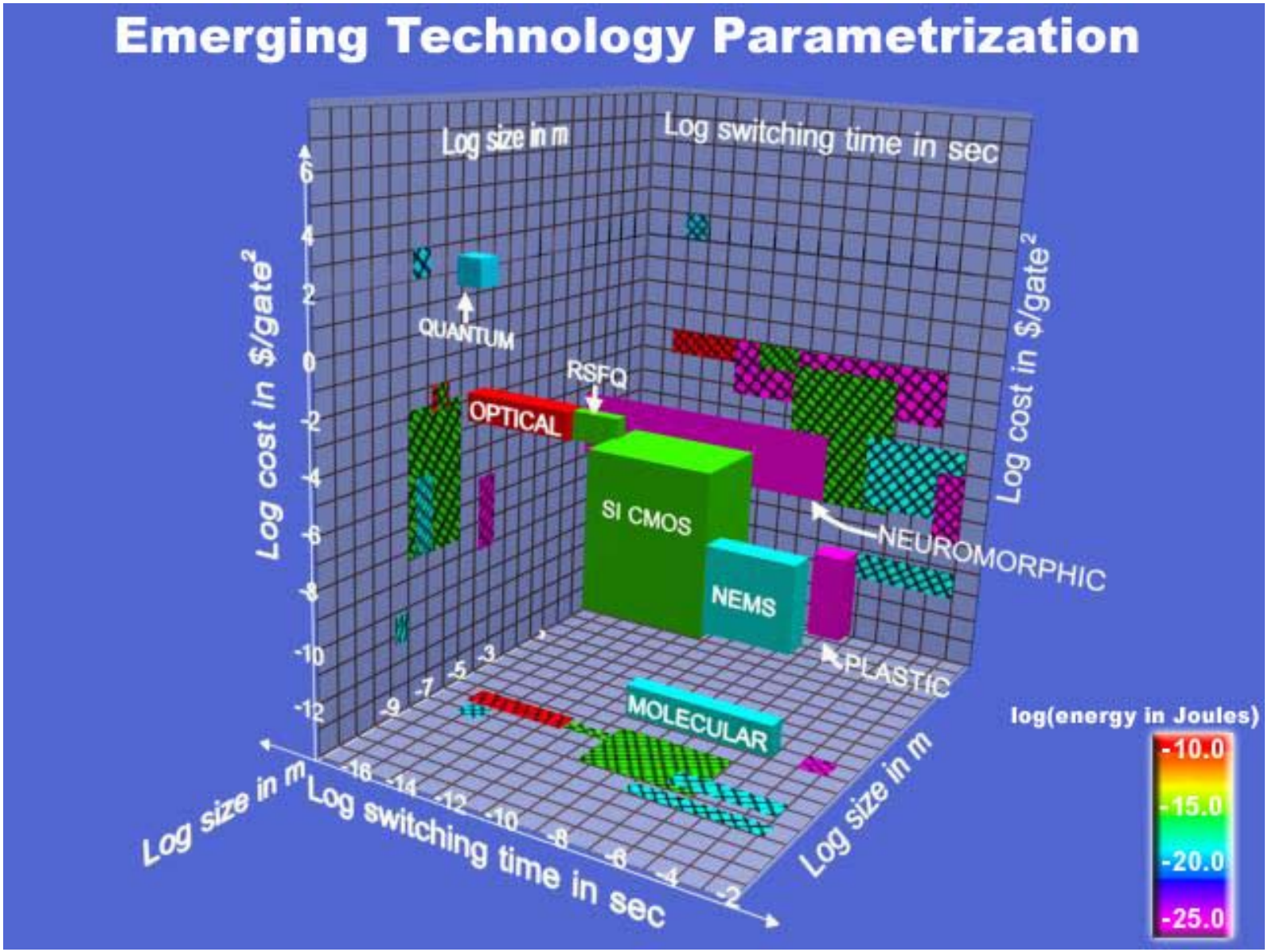
(see http://rsfq1.physics.sunysb.edu/~likharev/nano/GigaNano010603.pdf)

MOSFETS Below 10 nm: Quantum Theory

Konstantin K. Likharev – NanoMES 2003* – Tempe, AZ

- "Room-temperature devices with gate length (L_g) as short as 5 nm still have high transconductance and relatively small DIBL effects and thus may be suitable for nearly all digital applications. Moreover, transistors with L_g as small as 2.5 nm may still feature voltage gain above unity and hence may be the basis for digital electronics
- However, all characteristics of such devices are extremely sensitive to very small variations of their geometrical parameters (L_g, T_{Si} and T_{EOT}) as well as single charged impurities inside (or in the immediate vicinity of the channel)
- As a result of this sensitivity, fabrication of sub-10 nm devices with acceptable yield will require extremely tight specifications, far exceeding recent ITRS projections for the year 2016"

* To be published in Physica E (2003)

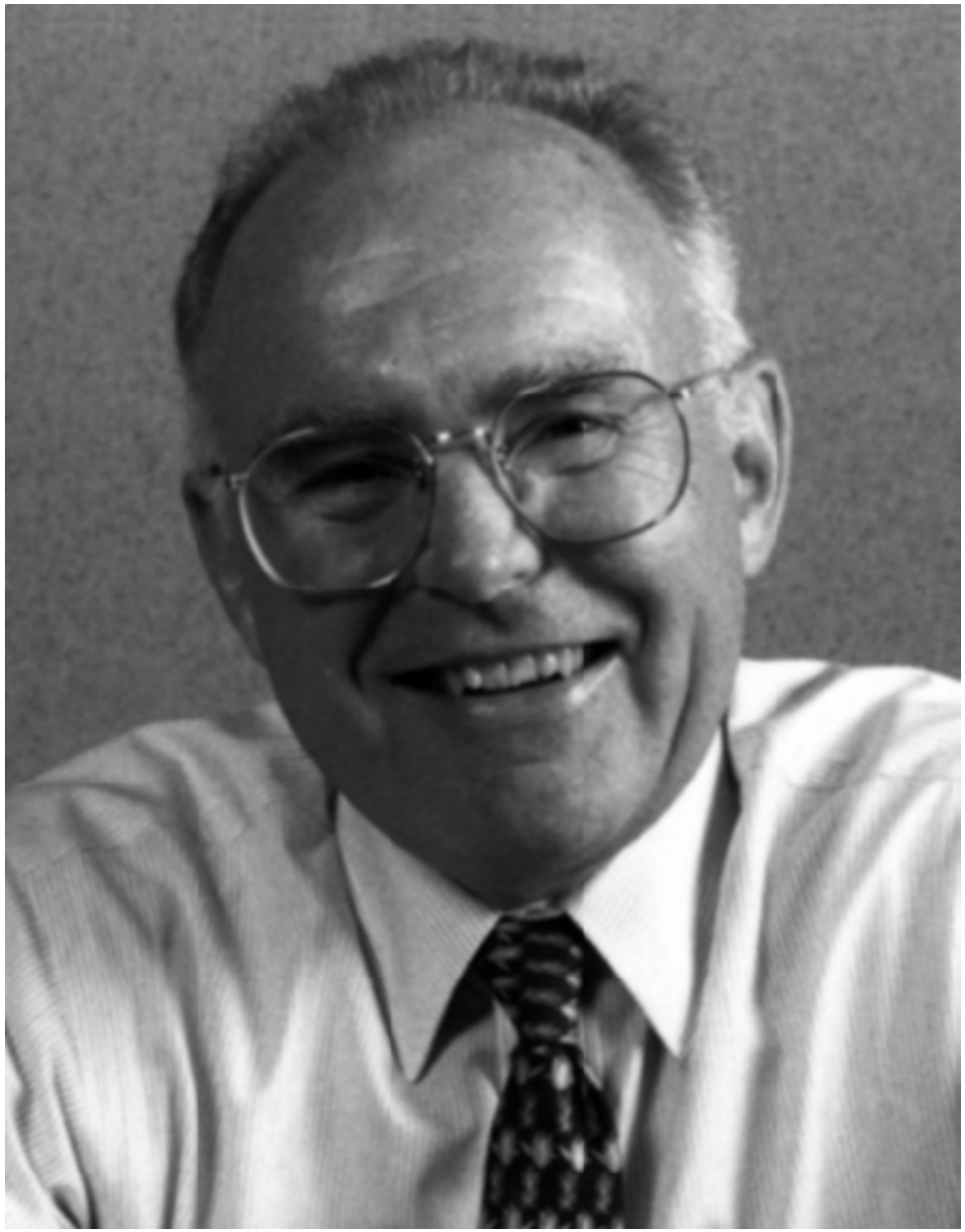

Emerging Technology Parametrization
Log size in m
Log switching time in sec
Log cost in $/gate²
QUANTUM
RSFQ
OPTICAL
SI CMOS
NEMS
NEUROMORPHIC
PLASTIC
MOLECULAR
log(energy in Joules)
-10.0
-15.0
-20.0
-25.0

Microelectronics Revolution

- **Gordon Moore (a)**
  - **"But then you see the numbers or hear your company's name on the evening news … and you are once again reminded that this is no longer just an industry, but an economic and cultural phenomenon, a crucial force at the heart of the modern world"**
- **Gordon Moore (b)**
  - **"No exponential is forever: but "forever" can be delayed!"**

(a) *Beyond Imagination:Commemorating 25 Years*, SIA (2002) [Introduction by Gordon Moore]
(b) ISSCC 2003 / Session 1/ Plenary 1.1 (2003)

Gordon Moore



John Bardeen

Courtesy of Lillian Hoddeson

Agenda

- Introduction
- Threshold events
- Transistor Fabrication
  - Point-contact
  - Grown-junction
  - Alloy formation
  - Diffusion
- Mesa and planar advances
- Integrated circuit beginnings
- Bipolar IC and DRAM IC Issues
  - (1960-1980's)
- Prognosis
- Acknowledgements

Acknowledgements

- **Presentation dedicated To Gordon K. Teal (1907-2003)**
- **We are indebted to the numerous industrial, university and government personnel, internationally, who have and continue to contribute to the content and formulation of the IC industry**